SPI-MS

Octal SPI Master/Slave Controller

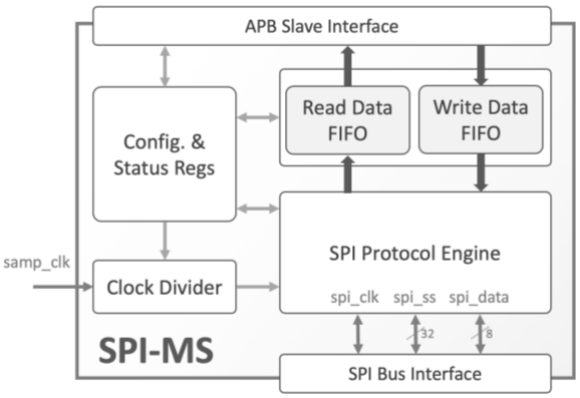
Implements a controller for a single-, dual-, quad-, or octal-lane Serial Peripheral Interface (SPI) bus, which can operate either as a master or as a slave.

Designed to work with a wide variety of SPI bus variants, the core supports run-time control of several SPI protocol parameters. For example, the SPI frame width can be 1 to 4 bytes, the most significant bit position in a frame, serial clock phase and polarity are all software-programmable. In master mode the core can control up to 32 slaves. A software controllable clock generator derives the serial clock for master mode, by dividing the frequency of a clock line dedicated for that purpose.

The SPI-MS provides access to is status and control registers, and to the SPI transfer data via a 32-bit APB slave interface. The core treats the APB and SPI clocks as asynchronous to each other, and implements a clean clock domain crossing boundary. The core implements two configurable-depth FIFOs, one for the receiver and one for the transmitter path. To ease integration, an interrupt can be generated to indicate availability of a programmable amount of received data or availability to transmit a programmable amount of new data.

The SPI-MS core is rigorously verified, silicon-proven and available in RTL source or as a targeted FPGA netlist.

Block Diagram



FEATURES

SPI I/O interface

- Compliant to the SPI de-facto standard
- Single, dual, quad and octal serial data lines
- Software programmable transmission formats (CPOL and CPHA)
- Up to 32 slaves supported under master control

Configurable SPI transfers

- Fast sampling clock input for the SPI transfers
- FIFOs used for transferring data (configurable depth)
- Full duplex operation
- LSB or MSB mode
- 8-bit, 16-bit, 24-bit and 32-bit synchronous serial transmission

APB interface

- Compatible with the APB3 protocol specification
- Software programmable Master or Slave mode
- Software programmable SCLK rate
- Interrupt control

Smooth Technology Mapping

- Fully synchronous, scan-ready, LINT-clean design
- Delivered with sample scripts, RTL testbench and sample test cases

Deliverables

- Synthesizable RTL or FPGA netlist
- Testbench & sample test cases
- Simulation & synthesis scripts
- Documentation

Size and Speed

The SPI-MS can be mapped to any ASIC technology or FPGA device (provided sufficient silicon resources are available). The following table provides sample implementation data. Please contact CAST to get characterization data for your target configuration and technology.

Configuration	Technology	Area (eq. Gates)	Clock Freq. (MHz)
Slave, Quad SPI	TSMC 16nm	3,657	APB: 500 SPI: 125
Master, Quad SPI		4,259	
Master & Slave, Octal SPI		4,641	

Verification

The core has been production proven in both ASIC and FPGAs. It has been rigorously verified through extensive synthesis, place and route, and simulation runs.

Support

The SPI-MS as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available

Applications

The SPI-MS core is suitable for implementing serial interfaces in a wide range of applications, including host communication with flash memories, and peripherals such as sensors, ADC/DACs, video game controllers, and audio/video codecs.

Deliverables

The core is available in synthesizable RTL and FPGA netlist forms, and includes everything required for successful implementation, including a testbench, simulation and synthesis scripts and comprehensive user documentation.