RTP2H264

Hardware RTP Stack for H.264 Stream Decapsulation

Implements a Real Time Transport Protocol (RTP) hardware stack that extracts H.264/NAL streams encapsulated in RTP packets.

The RTP2H264 core is compatible with RTP packets produced by CAST's H.264 to RTP encapsulation core (H2642RTP). The output of the RTP2H264 can be directly connected to the input of an H.264 decoder core. Along with CAST's UDP/IP hardware stack, the RTP2H264 core is ideal for offloading the demanding task of RTP/UDP/IP de-capsulation from a host processor, and enables H.264 video streaming even in processor-less SoC designs.

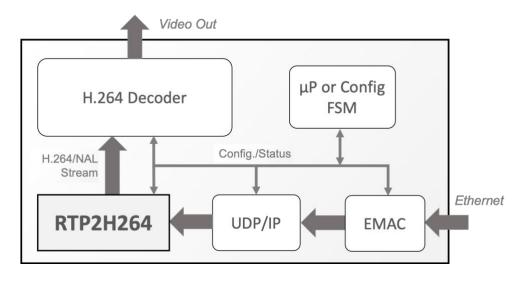
The core is easy to integrate in systems with or without a host processor. H.264 stream and RTP packet data are input/output via dedicated streaming-capable interfaces, enabling direct connection to hardware video encoders and hardware stacks for UDP or TCP. Status and control registers are accessible by an AXI4-Lite interface.

The RTP2H264 core is available in RTL source or as a targeted FPGA netlist. Platforms integrating the core along with H.264 decoder, UDP/IP, and eMAC cores, are also available from CAST, and can enable rapid development of video over IP systems.

Applications

The RTP2H264 core is suitable for a wide variety systems and devices featuring H.264 video streaming over IP networks. A sample block diagram of such systems is provided below.

Block Diagram



Support

The RTP2H264 as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

FEATURES

RTP Decapsulation for H.264 NAL Streams

- Compatible with RTP streams produced by CAST's H264 to RTP encapsulation core.
- Support for other RTP encapsulation stacks possible on request.

Easier Integration for Faster Development

- Processor-less, standalone operation
- AMBA® AXI Interfaces
- AXI4-Lite Control/Status register interfaces
- AXI4-Streaming interfaces for packet data
- Available preintegrated with:
 - H.264 Video Decoder cores from CAST
- UDP/IP Hardware Stack from CAST
- CAST, Intel, Xilinx, or other thirdparty eMAC core

Related Products

H264OIP-HDD: H.264 Over IP – HD Decoder Subsystem

<u>H2642RTP</u>: Hardware RTP Stack for H.264 Encapsulation

H264-LD-BP: Low-Power Baseline Profile Decoder

H264-D-BP: Low-Latency Baseline Profile Decoder

UDPIP: UDP/IP Hardware Protocol Stack

EMAC-1G: Gigabit Ethernet Media Access Controller

