PNG-E

PNG Lossless Compression Encoder Core

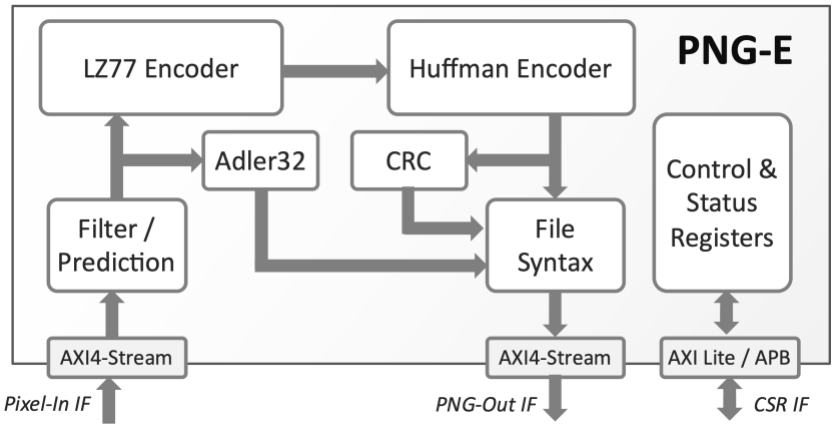
The PNG-E core implements a lossless image compression engine compliant with the Portable Network Graphics (PNG) file format specified in the ISO/IEC 15948 and RFC 2083 standards.

The encoder core can compress greyscale or truecolor (RGB) images, with 8 and 16 bits per color, with or without alpha transparency, and produces complete PNG files. It exhibits excellent compression efficiency thanks to its ability to automatically and dynamically choose the optimal prediction filter per line. It supports all four prediction filters, LZ77 with a configurable History Window, and Static Huffman tables, and it computes CRC and Adler32 checksums as provisioned by the standard. The core does not currently support the interlaced mode, Dynamic Huffman tables, and images with less than 8 bits per color, but these can be added on request.

The easy-to-use PNG-E core interfaces to the system via standardized AMBA® interfaces: it accepts images and outputs compressed data via AXI4-Stream interfaces and provides access to its control and status registers via a 32-bit APB interface. After its registers are programmed with the image dimensions and color format, the core can encode an arbitrary number of images without requiring any assistance or action from the system. The core provides one interrupt signal per direction to facilitate integration with a DMA engine. These interrupts are asserted when the input or output FIFO occupancy reaches a run-time programmable threshold.

Consistent with CAST's quality standards, the core was designed and verified using the industry's best practices, and is delivered with everything required for a trouble-free implementation.

Block Diagram



Applications

A wide range of SoC designs using PNG files can benefit from this custom-hardware compression engine's high performance and lower power. End applications range from wearables to data center acceleration and aerospace imaging.

Implementation Results

The PNG-E is a purely digital IP core and can be mapped on any Intel FPGA. The FPGA resources required for its implementation and the maximum clock rate depend on the core configuration. For a 512-byte history window, the core occupies approximately 4,500 ALMs and runs at 125MHz on a Arria 10 GX, -1 speed grade, device. Please contact CAST to get accurate characterization data for your target application and core configuration.

FEATURES

Efficient PNG Encoder

- Supports 8- and 16-bit greyscale, and 24- and 48-bit truecolor, with or without alpha transparency
- Outputs complete PNG files compliant with the ISO/IEC 15948 and RFC 2083 standards
- Optimizes the compression ratio by automatically selecting the best prediction filter for each line
- Implements all four prediction filters, LZ77 with a configurable history window, and Huffman encoding with static tables, and calculates Adler32 and CRC checksums

Easy to Use and Integrate

- Run-time programmable image format parameters
- Automatic program-once encode-many operation
- AXI4-Stream Interfaces for image and compressed data
- AXI-Lite or APB for control and Status register access
- Interrupts/DMA handshaking signals trigger based on programmable FIFO thresholds

Throughput & Latency

- One byte per cycle throughput
  - Higher throughput versions can be made available on request
- Ultra-low latency: one image line plus 40 clock cycles

Synthesis-Time Configuration Options

- Maximum image resolution and bytes per pixel
- LZ77 history window size
- Input & output FIFO depths

Deliverables

- LINT-clean Verilog RTL source code or targeted FPGA netlist
- Self-checking test-bench
- Bit-accurate software model
- Simulation & synthesis scripts
- IP-XACT register descriptions
- User documentation

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