PCI-M32

32-bit/33MHz PCI Master/Target Core

Microsemi

The PCI-M32 implements a master/target PCI interface compliant with the PCI 2.3 specification. It supports a 32-bit address/data bus and operates up to 33 MHz PCI clock.

The PCI-M32 Interface has both Master and Target capabilities. The interface implements 64 bytes of PCI Configuration Space registers. It is possible to extend the Configuration Space up to 256 bytes if required.

The Target part supports up to six Base Address Registers with both I/O and Memory space decoding from 16 bytes up to 2 GB. Both Target and Master supported commands are:

- Configuration Read, Configuration Write
- Memory Read, Memory Write, Memory Read Multiple (MRM), Memory Read Line (MRL)
- I/O Read, I/O Write

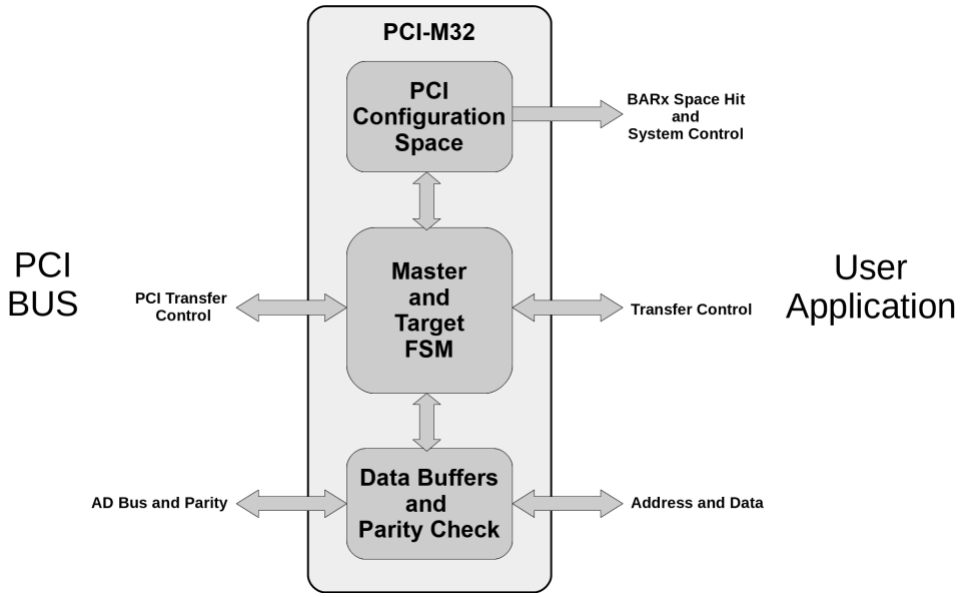
The PCI-M32 builds on more than 15 years of CAST PCI IP expertise and has been designed for straightforward reuse, with proven design practices that ensure easy integration and smooth technology mapping. The core is available in synthesizable RTL or as a targeted FPGA netlist, and is delivered with everything required for rapid and successful integration and implementation.

Applications

The PCI-M32 core can be utilized for a variety of applications including:

- PCI I/O communication boards
- PCI Data Acquisition Boards
- Embedded system PCI applications

Block Diagram



FEATURES

- PCI specification 2.3 compliant
- 33 MHz performance
- 32-bit datapath
- Zero wait states burst mode
- Full bus Master/Target functionality
- Single interrupt support
- Type 0 Configuration space
- Support of all Base Address Registers
- Support of backend initiated target retry, disconnect and abort
- Parity generation and parity error detection
- DMA Controller Core supporting independent write and read operations available
- Optional bridge / interface to AMBA/AHB

Implementation Results

PCI-M32 reference designs have been evaluated in a variety of technologies. The following are sample Microsemi results for the PCI-M32 core configured with two BARs, DMA and an ALU example application.

Microsemi Device	Cells		RAM Blocks	I/Os	Fmax (MHz)
	Sequ (R)	Comb (C)			
RadTolerant RTAX250S-1	620	1530	4	50	33
Axcelerator AX250-1	620	1530	4	50	33
SmartFusion2 M2S150-STD	848 DFF	1632 4LUT	9	50	33
Igloo2 M2GL150-STD	848 DFF	1632 4LUT	9	50	33

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core includes everything required for successful implementation:

- Post-synthesis netlist for PCI-M32 Core
- Post-synthesis netlist (firm core) for DMA Controller
- Sophisticated HDL Testbench
- Simulation script, vectors, expected results, and comparison utility
- Place and route script
- Comprehensive user documentation, including detailed specifications and a system integration guide

CAST PCI Cores Family

CAST offers a broad family of PCI cores the members of which along with their basic features are outlined in the following table.

	PCI-T32	PCI-T32MF	PCI-M32	PCI-M32MF	PCI-HB	PCI-HB-AHB	PCI-DHB-AHB
PCI 33 MHz	✓	✓	✓	✓	✓	✓	✓
Host	✗	✗	✗	✗	✓	✓	✓
Master	✗	✗	✓	✓	✗	✗	(✓)
Target	✓	✓	✓	✓	✗	✗	✓
Multifunction	✗	✓	✗	✓	✗	✗	✗
32bit	✓	✓	✓	✓	✓	✓	✓
64bit	✗	✗	✗	✗	✗	✗	✗
SoC Interface	Generic AXI, AHB, Avalon-MM[1]	Generic AXI, AHB, Avalon-MM[1]	Generic AHB, AXI, Avalon-MM[1]	Generic AXI, AHB, Avalon-MM[1]	Generic AXI, Avalon-MM[1]	AHB	AHB
ASIC Support	✓	✓	✓	✓	✓	✓	✓
FPGA Support	✓[2]	✓[2]	✓[2]	✓[2]	✓[2]	✓[2]	✓[2]

Notes:
- ✓ : Feature is supported
- (✓) : Feature optionally supported
- ✗ : Feature is not supported
- 1 : SoC interface in grey font can be made available upon request
- 2 : FPGA devices that do not support PCI I/O standard (e.g. Xilinx Virtex-6 and Stratix-V) are not supported