CAST NEWS

Data Compression Accelerators from CAST Now Available on Xilinx Alveo Boards

Reduce bandwidth and storage requirements with standard GZIP/ZLIB/Deflate compression at over 90Gbps on Xilinx Alveo Data Center Accelerator Cards

Woodcliff Lake, NJ — September 27, 2019 — Semiconductor intellectual property (IP) provider CAST, Inc. today announced that its GZIP/ZLIB/Deflate Compression and Decompression reference designs are now available on Xilinx® Alveo™ Data Center Accelerator Cards.

Already successfully deployed by multiple customers on Xilinx Kintex® and Virtex® Ultrascale FPGA boards, the GZIP-RD-XIL GZIP & GUNZIP Accelerator Reference Design now running on Xilinx Alveo PCIe cards delivers an unmatched combination of good compression ratio, low latency, and high throughout. As shown in Table 1, data compression at over 90 Gigabits per second (Gbps) is possible with the compression IP running on the mid-range Alveo U200 Card.

The company believes this industry-leading hardware compression combined with the complete Xilinx Alveo ecosystem makes the GZIP-RD-XIL one of the best-available options for reducing bandwidth and storage requirements in data centers and other data-heavy applications.

Board	Function	History Window	Huffman Tables	# Cores	C/R	Gbps	FPGA Resources			
							LUT	BRAM	URAM	DSP
KCU105	Compress	32k	Dynamic	1	3.74	1.0	87k	278	0	1
KCU105	Compress	16K	Dynamic	2	3.38	11.8	211k	562	0	2
VCU1525	Compress	32k	Dynamic	4	3.64	31.2	706k	1918	144	4
VCU1525	Compress	8K	Dynamic	4	3.38	76.1	869k	1156	216	8
ALVEO-U200	Compress	32k	Dynamic	4	3.49	42.8	757k	1694	224	8
ALVEO-U200	Compress	512	Dynamic	4	3.18	92.2	607k	1336	192	16
ALVEO-U200	Compress	1024	Static	4	2.35	94.0	634K	854	192	0
ALVEO-U200	Decompress	32k	Dynamic	4	N/A	27.0	130k	188	0	0
ALVEO-U200	Decompress	32k	Dynamic	8 (*)	N/A	42.0	193k	450	0	0

1. Table does not include all core's configuration parameters. The list of configurations is not exhaustive.
2. Compression ratio and throughput for Canterbury corpus.
(*) Decompression engine limited to operate on 64K files, and 2 cores per channel

Table 1. Representative configurations of the GZIP-RD-XIL reference design running on various Xilinx FPGA boards, with the key statistics of compression ratio (C/R) and performance (Gbps) highlighted.

About the GZIP Accelerator Reference Design

Sourced from partner Sandgate Technologies (www.sandgate.com), the lossless data compression and decompression engines in the reference design comply with the Deflate, GZIP, and ZLIB compression standards.

The ZipAccel-C Compression IP core offers a flexible architecture capable of extremely high throughput and latency as low as a few tens of clock cycles. The ZipAccel-D Decompression IP Core on average outputs three bytes of decompressed data per clock cycle with a latency of a few tens of clock cycles for blocks coded with static Huffman tables, or under 2,000 cycles for those with dynamic Huffman tables. Instances of the cores can be combined for easy scalability, and they are available for multiple ASIC and FPGA technologies.

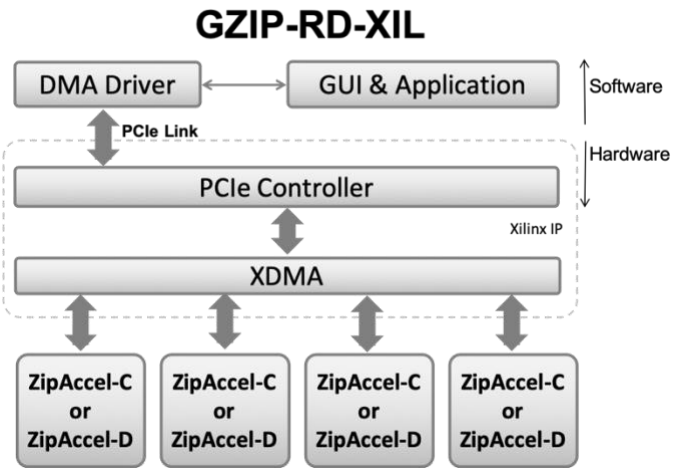

Figure 1. GZIP-RD-XIL compression or decompression reference design IP block diagram

The ZipAccel cores are part of CAST's broad IP portfolio, which includes 32- and 8-bit processors; hardware compression/decompression engines for data, images, and video; automotive and other interfaces and peripherals, and a comprehensive SoC security solution.

Learn more about the GZIP-RD-XIL GZIP & GUNZIP Accelerator Reference Design on Xilinx Alveo Cards and CAST's complete line of IP by visiting www.cast-inc.com, emailing info@cast-inc.com, or calling +1 202.891.8300.

CAST, Inc., 50 Tice Blvd, Suite 340, Woodcliff Lake, NJ 07677 USA • phone: +1 201.391.8300

# # #

Media Contact: Paul Lindemann, Montage Marketing, paul@montmark.com, +1 603.490.4985