CAST NEWS

Cache Controller Core from CAST Augments Cache-Less 32-bit Processors

WOODCLIFF LAKE, NEW JERSEY — September 19, 2016 — A cache memory controller IP core available from semiconductor intellectual property provider CAST, Inc. brings cost- and resource-effective improvements in performance, bandwidth, and function to systems using cache-less 32-bit processors.

The new CACHE-CTRL Cache Controller IP Core enables the addition of single or multilevel cache memory to systems using cache-less 32-bit processors such as the BA20 PipeLineZero™ or ARM® Cortex®-M0 processors. This can significantly decrease the access time to energy-consuming DRAM, Flash, or EEPROM memories. It also allows these economical processors to run code directly from an off-chip NOR-flash device (Execute in Place, XIP) while minimizing the typical performance or power penalties of off-chip access.

The Cache Controller is easy to add to general purpose, digital signal processing (DSP), or application-specific instruction set (ASIP) processors in different types of embedded systems. It uses standard AMBA® AHB processor and memory interfaces, and supports clock gating. Mapping the core to any ASIC or FPGA technology is straightforward, as it has no special static RAM requirements and works with any standard, single-ported SRAM device.

The Cache Controller supports a four-way associative cache memory, and implements a Least Recently Used (LRU) replacement policy. Users can configure the number of cache lines and cache line width at synthesis time. The core is conservative in its use of silicon area; for example, when configured with eight words per line and 256 lines per set (1024 lines in total), it synthesizes to about 9,000 equivalent NAND2 gates. It also performs well—running over 1GHz in a typical 20nm technology—and has been silicon-proven.

Sourced from Silesia Devices, the new Cache Controller Core is available now from CAST. See www.cast-inc.com, email info@cast-inc.com, or call +1 201.391.8300 for more information. # # #

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