MM2ST

AHB/AXI4-Lite to AXI4-Stream Bridge

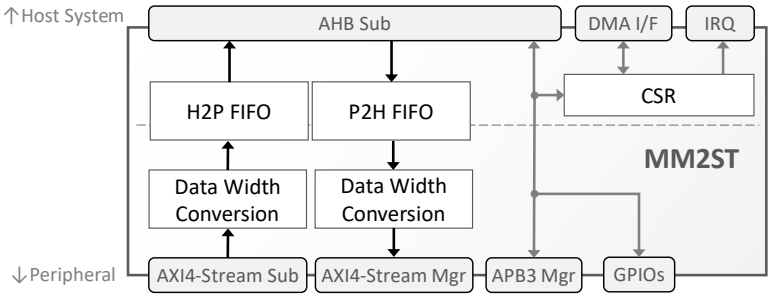
The MM2ST IP core bridges the streaming interfaces of a peripheral or accelerator to a memory-mapped AMBA® AHB or AXI4-Lite bus.

The bridge core connects to the peripheral via four interfaces: an AXI4-Stream interface per direction, each with a configurable data width; a configurable number of general-purpose input and output (GPIO) pins; and, optionally, a 32-bit-wide APB3 interface for accessing the peripheral's Control and Status Registers (CRS). The MM2ST connects to the host system via its 32-bit or 64-bit wide AHB or AXI4-Lite subordinate port, an interrupt line, and direct memory access (DMA) controller handshaking signals.

Designed for ease of integration, it optionally implements clean clock-domain crossing (CDC) boundaries, allowing the peripheral and host system to operate in different clock domains.

The MM2ST core is rigorously verified, LINT-clean, and scan-ready. It is available in synthesizable Verilog and FPGA netlist forms and ships with everything required for successful implementation, including a testbench, simulation, and synthesis scripts, and comprehensive user documentation.

Block Diagram



Applications

The MM2ST core can be used in any SoC integrating streaming-capable peripherals that need to receive input or store outputs via a memory-mapped bus. Examples include compression, video, or packet processing engines. The core is an excellent companion to CAST's data compression, video or image codecs, IP stacks, or cryptography cores.

Performance and Size

The MM2ST core is a purely digital design and can be mapped to any Intel FPGA. The following table provides sample implementation results for an Arria1-GX device and all clocks constrained to 300MHz.

Configuration	Logic Resources (ALMs)	Memory Resources (Block Mem. bits)
32-bit AHB, 16-bit AXI4-Stream P2H & H2P, 32 GPIOs, 8-words deep CDC FIFOs,16-words deep data FIFOs	690	1,712
32-bit AHB, 32-bit AXI4-Stream P2H & H2P, 64 GPIOs, 8-words deep CDC FIFOs, 16-words deep data FIFOs	680	1,712
32-bit AHB, 256-bit AXI4-Stream P2H & H2P, 64 GPIOs, 8-words deep CDC FIFOs, 256-words deep data FIFOs	1,268	18,752

These sample implementation figures do not represent the highest speed or smallest area possible for the core. Please contact CAST to discuss silicon resource utilization and performance for your target configuration and technology.

Support

The MM2ST as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

FEATURES

Memory-Mapped to Stream Bridge

- Bridges AXI4-Stream and APB register interfaces of a peripheral to a 32-bit or 64-bit AHB or AXI-Lite subordinate port
- Optionally implements clean CDC boundaries between the peripheral and the host bus clocks
- Performs data-width conversion from/to the peripheral's buses data widths to/from the width of the memory mapped bus

Interfaces

- Host Interface:
  - 32-bit or 64-bit AHB or AXI4-Lite Subordinate
  - Interrupt with maskable sources
- Peripheral Interface
  - A configurable-width (up to 512 bits) AXI4-stream per direction
  - 32-bit APB interface for CSR access
  - Configurable number of GPIOs
- Handshaking signals for external DMA controller

Synthesis-Time Configuration Options

- Data width for the AXI-Stream interfaces
- Data width of the memory-mapped interface (32 or 64 bits)
- Number of general-purpose input and output pins
- AHB address width
- Instantiation of the APB manager port
- APB address offset and width
- Instantiation of CDC logic
- FIFO sizes

Deliverables

- Synthesizable RTL or FPGA netlist
- Verilog testbench & sample test cases
- Simulation & synthesis scripts
- Documentation

www.cast-inc.com • info@cast-inc.com