MC-SDMA

Multi-Channel Streaming DMA Controller

The MC-SDMA IP core implements a highly configurable, bandwidth-efficient, and easy-to-use Direct Memory Access (DMA) controller that transfers data between the host system's memory and multiple peripherals equipped with streaming interfaces.

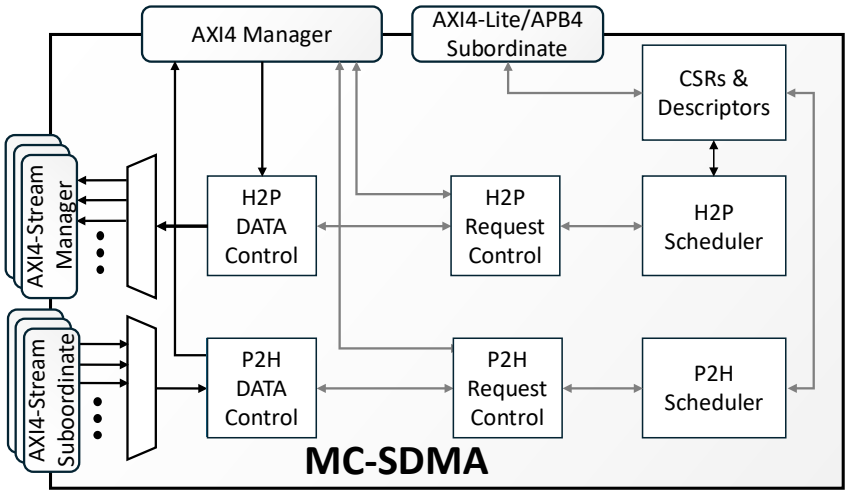
The core interfaces with the host memory via a manager AMBA® AXI4 (memory-mapped) port and provides access to its configuration and status registers (CSRs) via a subordinate AXI4-Lite or APB4 interface. Peripherals can be connected to the DMA controller via a configurable number of manager and subordinate AXI4-Stream interfaces, enabling both Host-to-Peripheral (H2P) and Peripheral-to-Host (P2H) data transfers.

Descriptors, one for each channel, are programmed with details of the data transfers through the CSR interface. Details include source (H2P) and destination (P2H) addresses, transfer size up to 2 GBytes, and control information. To further enhance workload handling, the MC-SDMA allows transfers to be split into smaller blocks. After each block's transfer, the core arbitrates between competing DMA requests, enabling transfer interleaving and efficient bandwidth allocation. A number of memory locations can also be skipped after the transfer of each block of data, enabling the transfer of images, video frames, or graphics elements with a single descriptor. In the P2H direction, descriptors are updated with the actual transfer size—in case the peripheral asserts TLAST early—and with the value of the sideband TUSER bus. The H2P descriptors can enable the assertion of TLAST at the end of the transfer and control the value of the TUSER bus.

The MC-SDMA is highly configurable both at synthesis and runtime, allowing it to be tailored to specific application requirements. Synthesis parameters include the number of P2H and H2P channels, instantiation and sizing of FIFOs, and address and data-bus widths. Runtime programmability includes channel priority order, maximum transfer burst length, and interrupt triggers.

The MC-SDMA core is rigorously verified, LINT-clean, and scan-ready. It is available in synthesizable Verilog and FPGA netlist forms and includes everything required for successful implementation, including a UVM testbench, simulation, and synthesis scripts, and comprehensive user documentation.

Block Diagram



FEATURES

- DMA controller transfers data between host memory and peripherals with streaming interfaces
- Optionally supports memory-to-memory transfers with loop-back between an H2P and a P2H channel

Highly configurable

- Synthesis-time parameters:
  - Number of P2H and H2P channels (up to 16 per direction)
  - Data-bus width (32–1024 bits) and address-bus width (32–64 bits)
  - TUSER bus width (0–32 bits)
  - CSRs reset values
  - FIFO sizes and instantiation
  - Separate CSR clock domain with clock domain crossing (CDC)
- Runtime parameters:
  - AXI4 burst size
  - Channel priority order
  - Interrupt triggers
  - Transfer descriptor format

Efficient bandwidth utilization

- Access requests pipelining
- Interleaving large transfers with split transfer option
- Programmable channel priority

Easy to use and integrate

- Configurable-width AXI4 manager interface towards the system memory
- Configurable-width AXI4-stream manager and/or subordinate interfaces towards the peripherals
- TLAST behavior control for H2P transfers
- Early terminated transfer reporting for P2H transfers
- TUSER value control (H2P) and capture (P2H) via CSR
- Configurable-width AXI4-Lite or APB4 subordinate interface for control and status registers (CSR) access.
- Hardware-triggered and software-triggered transfers
- Add-on CRC or checksum modules and data-width converters optionally available

Optional Functional-Safety features:

- Core can compute and report transfer data checksums
- CSRs and FIFOs can on-request be parity-protected

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Applications

The MC-SDMA is suitable for applications requiring high-speed data transfers and efficient host memory access. Examples include networking equipment for handling packet data, multimedia systems for managing audio/video streams, storage systems for accelerating data movement, and embedded systems for optimizing resource usage in IoT or automotive applications.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty-days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available

Deliverables

The core is available in synthesizable HDL (SystemVerilog) or targeted FPGA netlist forms and includes everything required for successful implementation. Its deliverables include:

- Sophisticated UVM-based test environment.
- Software bit-accurate model and test vector generator.
- Simulation and synthesis scripts.
- Comprehensive user documentation.
- IP-XACT register descriptions.