LZ4SNP-D

LZ4/Snappy Data Decompressor

LZ4SNP-D is a custom hardware implementation of a lossless data decompression engine for the LZ4 and Snappy compression algorithms. The core receives compressed files, automatically detects the LZ4 or Snappy format, and outputs the decompressed data.

The core features fast processing with low latency and high throughput. In its default configuration, LZ4SNP-D outputs up to 7.8 bytes of decompressed data per clock cycle and can be clocked at frequencies exceeding 300MHz on Kintex UltraScale+ devices. Designers can scale the throughput by instantiating the core multiple times to achieve throughput rates exceeding 100Gbps. The processing latency is approximately 30 clock cycles.

The decompression core operates on a standalone basis—offloading the host CPU from the demanding task of data decompression—and has been designed for easy integration and use. No preprocessing of the incoming compressed files is required, as the core parses the file headers, checks the input files for errors, and outputs the decompressed data payload.

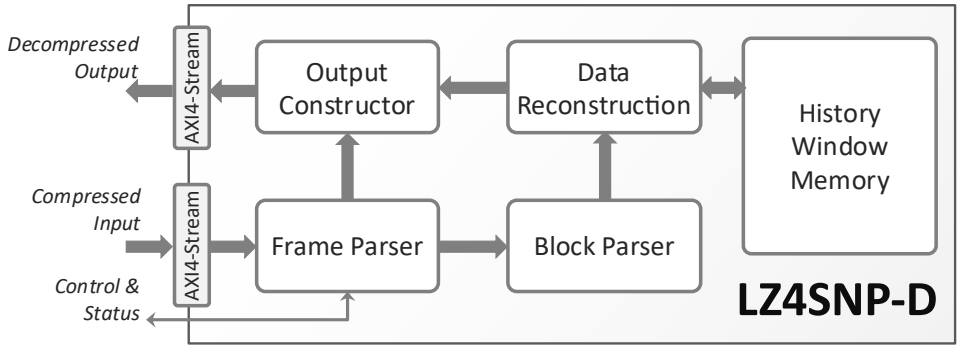
Extensive error tracking and reporting enable the core to ensure smooth system operation and error recovery, even in the presence of errors in the compressed input files. Furthermore, internal memories can optionally support Error Correction Codes (ECC) to simplify achieving enterprise-class reliability or functional safety requirements.

The LZ4SNP-D core is a microcode-free design developed for reuse in ASIC and FPGA implementations. Its streaming data interface—optionally bridged to AMBA® AXI4-Stream—eases SoC integration. Technology mapping is straightforward, as the design is scan-ready, LINT-clean, microcode-free, and uses easily replaceable, generic memory models.

Applications

Supporting high-speed decompression of data compressed using either the LZ4 or Snappy algorithms, the LZ4SNP-D core is well-suited for a range of applications where fast data retrieval and low-latency decompression are critical. This includes embedded systems, network devices, edge/cloud accelerators, datacenter storage solutions, and real-time data streaming applications, where efficient bandwidth usage and rapid access to compressed content can significantly enhance system performance. Its ability to handle both LZ4 and Snappy formats makes it particularly versatile for interoperability with widely-used compression standards. The LZ4SNP-D core is an ideal complement to CAST's LZ4SNP-C IP core, which performs high-speed compression in the same formats, enabling end-to-end hardware-based compression and decompression solutions that are both fast and resource-efficient.

Block Diagram



FEATURES

Dual-Format Decompression

- LZ4
  - 64KB history window size
  - All frame and block formats
  - CRC checking (optional, on request)
  - Dictionaries not supported
- Snappy
  - 64KB history window size
  - All frame and stream formats
  - CRC checking (optional, on request)

High Performance & Low Latency

- Processing rate up to 7.8 decompressed bytes per clock cycle
- Clock frequency in excess of 300MHz for Kintex UltraScale+ devices
- Latency of approximately 30 clock cycles

Easy to Use and Integrate

- Processor-free, standalone operation
- Automatic detection of input frame format (LZ4 or Snappy)
- Extensive error catching & reporting for smooth operation and recovery in the presence of errors
  - CRC 32 errors
  - File size errors
  - Coding errors
  - Non-correctable ECC memory errors
- Optional ECC memories
- AXI-Stream or native FIFO-like data interfaces
- Single clock domain design
- Interface bridges and DMAs available separately
- Microcode-free, LINT-clean, scan-ready design

Configuration Options

- Synthesis-time configuration options allow finetuning the core's size and performance:
  - Input and output bus widths
  - FIFO sizes
  - Maximum history window
  - Data-path width
  - more

Performance and Area (AMD)

LZ4SNP-D can be mapped on any AMD FPGA, and its resource requirements and throughput depend on its configuration. Also, its performance can scale via multiple core instances.

The following table provides sample FPGA resource utilization data for the core mapped on an Artix Ultrascale+ device with its clock set to 300MHz.

Datapath Width (bits)	LZ4 Support	Snappy Support	Max. History	Logic Resources (LUTs)	Memory Resources (RAMB)
32 bits	Yes	No	64kB	3,377	19
32 bits	No	Yes	64kB	3,010	19
32 bits	Yes	Yes	64kB	4,114	19
64 bits	Yes	No	64kB	4,307	20
64 bits	No	Yes	64kB	3,929	20
64 bits	Yes	Yes	64kB	5,105	20

Please contact CAST Sales to get accurate characterization data for your target FPGA device and configuration.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available in synthesizable HDL (System Verilog) or targeted FPGA netlist forms and includes everything required for successful implementation. Its deliverables include:

- Sophisticated Test Environment
- Simulation scripts, test vectors, and expected results
- Synthesis script
- Comprehensive user documentation

Related Cores

- LZ4SNP-C: LZ4/Snappy Data Compressor
- AXI4-SGDMA: AXI4 to/from AXI4-Stream Scatter-Gather DMA Controller
- MC-SDMA: Multi-Channel Streaming DMA
- MM2ST: AHB/AXI4-Lite to AXI4-Stream Bridge
- ZipAccel-D: GZIP/ZLIB/Deflate Data Decompressor
- ZipAccel-C: GZIP/ZLIB/Deflate Data Compressor