LIN

LIN Bus Master/Slave Controller

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SEMICONDUCTOR™

The LIN core is a communication controller that transmits and receives complete LIN frames to perform serial communication according to the LIN Protocol Specification. The LIN controller can be implemented as a master or as a slave and operate on LIN 1.3, 2.0, 2.1 or 2.2 LIN network. It uses a single master/multiple slave concept for message transfer between nodes of the LIN network. The message transfer can be controlled via a micro controller interface and a LIN transceiver is needed for the connection to the LIN bus.

The LIN core is a microcode-free design developed for reuse in ASIC and FPGA implementations. The scan-ready design is strictly synchronous with positive-edge clocking and no internal tri-states. The robustly verified core has been production proven multiple times.

Applications

The LIN core is used to interface sensors and actuators in a variety of applications such as automotive, industrial and home appliances.

Block Diagram
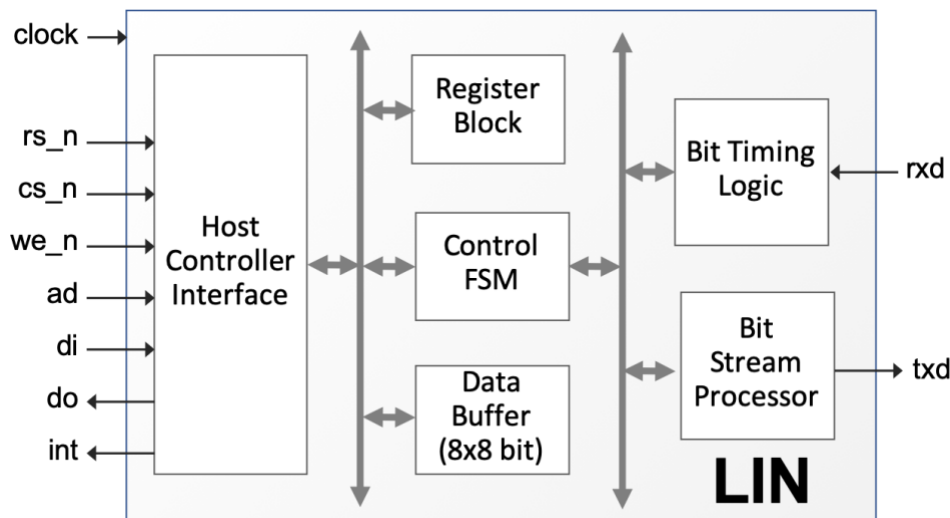
Functional Description

The LIN core is partitioned into modules as shown in the block diagram.

Host Controller Interface

This interface is responsible for handling the communication with the host controller of the system.

Register Block

The Register Block provides control registers and status registers to control the LIN message transfer. Access to the registers is possible via the host controller interface.

Data Buffer

The 8-byte Data Buffer stores the data that has to be sent with the current LIN frame or the data that has been received with the last LIN frame. Access to the Data Buffer is possible via the host controller interface.

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Functional Description (cont.)

Control FSM

The finite control state machine is responsible for the behavior of the core depending on host controller commands and bus activity. It generates and processes the LIN frame fields according to the LIN protocol.

Bit Stream Processor

This module converts the data stream from parallel to serial (from transmit buffer to bus) and from serial to parallel (from bus to receive buffer).

Bit Timing Logic

The Bit Timing Logic is responsible for synchronizing the received data stream from the bus with the internal bit time clock.

Implementation Results

The LIN core can be mapped to any Lattice Device (provided sufficient silicon resources are available) and optimized to suit the particular project's requirements. The following are sample implementation data for the core assuming all I/Os are routed off-chip.

Family	Device	Config	Logic	Fmax[2] (MHz)
MachXO2	7000HC-5	Master	269 Slices 536 LUT4s	68
MachXO2	7000HC-5	Slave[1]	419 Slices 836 LUT4s	55

Notes:
1) Slave implemented with clock synchronization
2) Working frequency of LIN controller is 4 MHz

Core Modifications

The LIN core can be modified to include an acceptance filter. With that, a simple LIN slave that transmits response frames for only one identifier could be realized without the assistance of a host controller.

Please contact CAST, Inc. directly for any required modifications.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive synthesis, place and route, and simulation runs. It has been embedded in several shipping customer products, and is proven in both ASIC and FPGA technologies.

Deliverables

The core is available in synthesizable RTL and FPGA netlist forms, and includes everything required for successful implementation, including a sophisticated self-checking testbench, simulation scripts, test vectors, expected results, synthesis scripts and comprehensive user documentation.

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