L8051XC

Legacy-Configurable 8051-Compatible Microcontroller

intel FPGA

The L8051XC1 core implements an MCS®51-compatible microcontroller that is specially designed to match the timing and peripherals of legacy 8051 MCU based systems.

The core can be configured to execute an instruction every 12, 6, or 4 clock cycles. Architectural extensions are user-selectable, including multiple data-pointers, a multiply-division unit, and a power management unit. Furthermore, the 8051 CPU can be coupled with a wide range of peripherals matching the behavior and timing of peripherals found in legacy architectures from Intel® and others. Several pre-configured versions are offered; custom variations are also available.

The L8051XC1 runs legacy code, but new software development is facilitated through CAST's on-chip debugging option, and debug pods that cooperate with IAR Embedded Workbench & Keil uVision™ IDEs.

This product builds on CAST's experience with hundreds of 8051 IP customers going back to 1997. Designed for easy reuse in ASICs or FPGAs, the core is strictly synchronous, with positive-edge clocking (except in the optional debug & SPI modules), synchronous reset, and no internal tri-states. Representative Cyclone-IV results show the core to be conservative in its use of FPGA resources, requiring just 2,000 to 11,500 LEs.

Applications

The L8051XC1 MCU core is especially effective for extending the lifetime of existing systems where an originally-used discrete 8051 chip is difficult to replace, or the designer wishes to consolidate a multi-board system into a single FPGA or ASIC.

Block Diagram
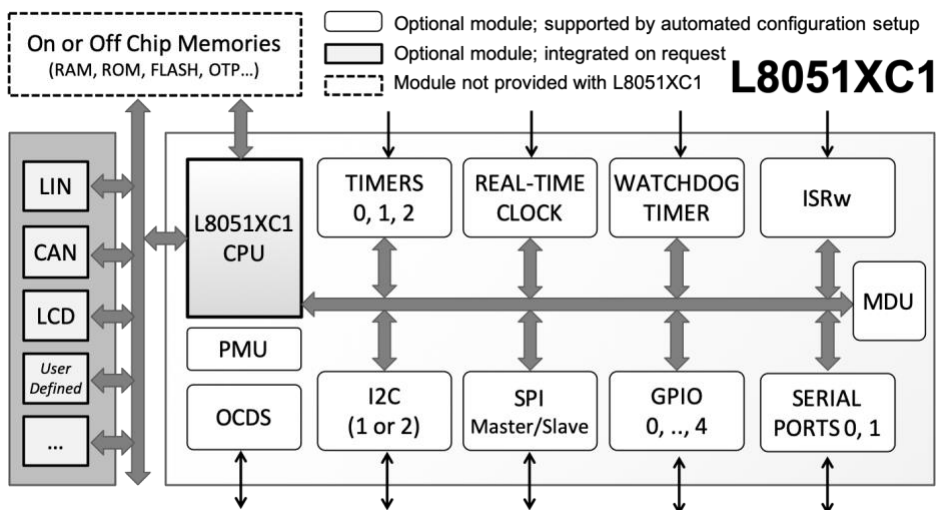
FEATURES

- Fully compatible with the MCS® 51 instruction set
- Configurable CPU architecture: 12, 6, or 4 clock cycles per machine cycle
- Extensive set of optional features and peripherals
- JTAG-based On-Chip Debug Support (OCDS)
- Integration with IAR Embedded Workbench & Keil uVision™ IDEs

Options and Peripherals

A wide range of architectural options and peripherals is available for integration with the L8051XC1, and more peripherals can be developed on demand. The following is partial list of the off-the-shelf available peripherals:

- External Memory Interface:
  - One, two or eight Data Pointers for fast data block transfer
  - Additional Arithmetic Unit supports data pointers, auto-increment/-decrement, and auto-switch
  - Supports external DMA controller through HOLD function
  - Program memory write mode
- Direct Memory Access (DMA) Controller
- Multiplication-Division Unit
- 37 to 119 external Special Function Registers
- Interrupt Controller with two or four priority levels, and six or eighteen interrupt sources
- Up to five Parallel I/O Ports
- Serial 0 full-duplex serial interface (80C51-like), equipped with an additional baud rate generator
- Serial 1 (asynchronous-only version of Serial 0) interface
- SPI Master/Slave interface
- One or two I2C™ Master/Slave interfaces
- Timers 0, 1 and Timer 2 with Compare/Capture(80C515-like)
- 15-bit programmable Watchdog Timer
- Real Time Clock
- Power Management Unit with power-down modes (IDLE/STOP)

Available Versions

Three standard versions of the core are available, offering a range of capabilities and prices.

- **L8051XC1-A** includes options that match the original Intel® 8051 peripheral set: 64KB memory interface, two timers, one serial port, four parallel I/O Ports, two-level interrupt controller, and two DPTR registers. These options are user-configurable (i.e., may be deleted prior to synthesis).

- **L8051XC1-B** includes options that match the Infineon 80515/80517 peripheral set: 64KB memory interface, three timers, two serial ports, four parallel I/O ports, watchdog timer, multiplication-division unit, and two DPTR registers. These options are user-configurable (i.e., may be deleted prior to synthesis).

- **L8051XC1-C** has custom/user-defined architectural and peripheral options. This version may integrate user-defined peripherals that are not supported by the automatic configuration tool. Please consult with your CAST sales contact to discuss your specific requirements and get lead time information

ASIC (RTL) and FPGA (netlist) deliverables are available; FPGA packages are not user-configurable.

Implementation Results

L8051XC1 designs have been evaluated in a variety of technologies. The following are sample Intel® results that are obtained after speed optimization during synthesis and place and route, while assuming that all core I/Os are routed off-chip.

Table 1: Sample Implementation results for CycloneIV-C6

Configuration	Logic Utilization (LEs)	Fmax (MHz)
L8051XC1-CPU (CPU-only)	1,932	90
L8051XC1-A (Timer 0 & 1, Serial 0, 4 parallel ports)	2,684	75
L8051XC1-CF (Timer 0, 1 & 2, WDT, RTC, SPI, 2 I2C, Serial 0 & 1, 4 parallel ports, MDU, DMA, 8 DPTRs, DPTR Arith, OCDS)	11,532	51

Table 2: Sample Implementation results for CyloneV-C8

Configuration	Logic Utilization (ALUTs)	Fmax (MHz)
L8051XC1-CPU (CPU-only)	1,287	76
L8051XC1-A (Timer 0 & 1, Serial 0, 4 parallel ports)	1,814	68
L8051XC1-CF (Timer 0, 1 & 2, WDT, RTC, SPI, 2 I2C, Serial 0 & 1, 4 parallel ports, MDU, DMA, 8 DPTRs, DPTR Arith, OCDS)	8,498	43

The provided figures <u>do not </u>represent the higher speed or smaller area for the core and area figures do not include any memories.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available; contact CAST Sales.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements. All subcomponents were functionally verified with an HDL testbench using their individual test suites. The CPU and ALU have been verified against a proprietary hardware modeler and behavioral models. The peripherals have also been verified in their own testbenches, based on either hardware or behavioral models. An extensive constrained random verification was performed to verify the CPU, DMA and OCDS.

Deliverables

The core is available in ASIC (synthesizable HDL) or FPGA (netlist) forms, and includes everything required for successful implementation. ASIC versions include:

- HDL RTL source code
- Easy-to-use configuration tool (with configurable versions)
- An example chip implementation, which uses the core in a sample system
- Sophisticated self-checking HDL Testbench including everything needed to test the core (Verilog versions use Verilog 2001)
- Simulation script, vectors, and expected results
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide

A reference design board is available; contact CAST Sales for information.

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