JPEG-EX-F

Ultra-Fast Baseline and Extended JPEG Encoder

This JPEG compression IP core supports the Baseline Sequential DCT and the Extended Sequential DCT modes of the ISO/IEC 10918-1 standard. It implements a scalable, ultra-high-performance, ASIC or FPGA, hardware JPEG encoder that can compress high pixel rate video using significantly fewer silicon resources and less power than encoders for video compression standards such as HEVC/H.265, DSC, AVC/H.264, or JPEG200.

The JPEG-EX-F encoder produces compressed JPEG images and the video payload for Motion-JPEG container formats. It accepts images with up to 12-bit color samples and up to four color components, in all widely-used color subsampling formats.

Depending on its configuration, the encoder processes from two to 32 color samples per clock cycle, enabling it to compress UHD (4K/8K) video and/or very high frame video.

Once programmed, the easy-to-use encoder requires no assistance from a host processor to compress an arbitrary number of frames. SoC integration is straightforward thanks to standardized AMBA® interfaces: AXI Streaming for pixel and compressed data, and a 32-bit APB slave interface for registers access. Users can optionally insert timestamps or other metadata in the compressed stream using a dedicated AXI Streaming interface.

Customers with a short time to market priority can use CAST's IP Integration Services to receive complete JPEG subsystems. These integrate the JPEG encoder with video interface controllers, Hardware UDPIP or Transport Stream networking stacks, or other IP cores available from CAST.

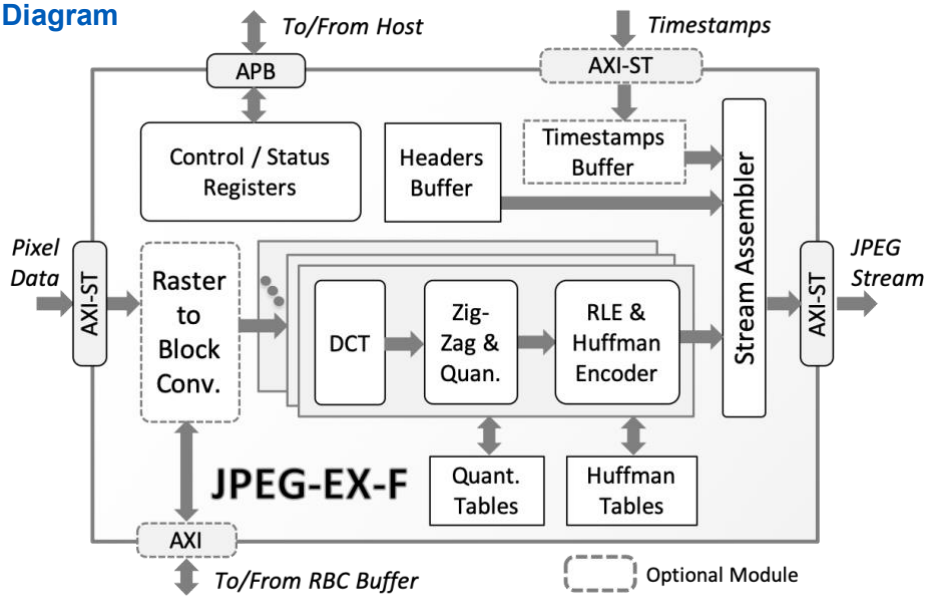
The core is designed with industry best practices, and its reliability and low risk have been proven through both rigorous verification and customer production. Its deliverables include a complete verification environment and a bit-accurate software model.

Applications

The JPEG-EX-F core is suitable for systems supporting ultra-high frame resolutions and/or frame rates, such as:

- Corporate, airborne, and other security or surveillance systems.
- Machine vision and video link decoders or terminals for industrial, or defense systems.
- Medical imaging systems.

Block Diagram



FEATURES

Scalable, ultra-high performance 4K/8k capable JPEG Encoder

- Requires significantly lower power and fewer silicon resources than any equally fast hardware video encoder for HEVC/H.265, AVC/H.264, DSC, or JPEG2000.
- Consumes much less power than any equivalent software, or software-hardware encoder.

Standards Support

- ISO/IEC 10918-1 Baseline and Extended Sequential DCT modes
- Single-frame JPEG images and Motion JPEG payloads
- 8-bit and 12-bit per color samples
- Up to four color components; any image size up to 64k x 64k
- All scan configurations and all JPEG formats APP, COM, and restart markers
- Programmable Huffman and Quantization tables

Rate Control Options

- Image: Limits the size of each individual frame
- Video: Regulates bit rate over a number of input frames.

Interfaces

- AXI Streaming pixel and compressed stream interfaces
- APB Control/Status interface

Performance

- Synthesis-time configurable scalable throughput
- Up to 32 samples per clock cycle
- Supports UHD (4k/8K) video and/or ultra-high frame rates

Ease of Integration

- Automatic program-once/encode-many operation
- Simple, dedicated timestamps interface
- Bit-accurate software model generates test vectors, expected results, and core programming values
- Optional Raster-to-Block Conversion with AXI or standard memory interface to the lines buffer

www.cast-inc.com • info@cast-inc.com • tel +1 201.391.8300

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Silicon Resources Utilization

The JPEG-EX-F core can be mapped to any ASIC and optimized to suit the particular project's requirements. The following table provides sample implementation and performance data with the core configured to process 2 pixels per cycle (JPEG-EX-F/2) and under its default configuration.

JPEG-EX-F/2	UHD/4k 60 fps 4:2:2	UHD/4k 120 fps 4:2:0	UHD/4k 120 fps 4:2:2	Area (Kgates)	Freq (MHz)
TSMC 40g	✔	✘	✘	145	500
TSMC 28hpm	✔	✔	✘	120	800
TSMC 16	✔	✔	✔	130	1,000

Note that the list of video formats is not exhaustive, and that these sample implementation figures do not represent the highest speed or smallest area possible for the core. Please contact CAST to discuss silicon resource utilization and performance for your target technology.

Verification

The core has been verified through extensive synthesis, place and route and simulation runs. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- Verilog RTL source code
- Sophisticated self-checking Testbench
- Software (C++) Bit-Accurate Model
- Sample simulation and synthesis scripts
- Comprehensive user documentation

JPEG Cores Available from CAST

This core is one member of the family of JPEG encoder and decoder cores that CAST offers. The following table summarizes the family members and indicates their basic features.

JPEG IP Cores	JPEG-E-T Tiny Baseline JPEG Encoder	JPEG-E-S Baseline JPEG Encoder	JPEG-EX-S Extended JPEG Encoder	JPEG-EX-F Ultra Fast Ext. JPEG Encoder	JPEG-D-S Baseline JPEG Decoder	JPEG-DX-S Extended JPEG Decoder	JPEG-DX-F Ultra Fast Ext. JPEG Decoder
Functionality	Encoder				Decoder		
Baseline JPEG	✔	✔	✔	✔	✔	✔	✔
Extended Sequential JPEG	✘	✘	✔	✔	✘	✔	✔
Motion JPEG Payload	✔	✔	✔	✔	✔	✔	✔
Sub-sampling Formats	Any with up to four components including Single–color, 4:4:4, 4:2:2, 4:2:0						
Image Resolution	16x16 to 64k x 64k						
Max. Sample Depth	8	8	12	12	8	12	12
Programmable Huffman Tables	✘	✔	✔	✔	N/A	N/A	N/A
Rate Control	✘	✔	✔	✔	N/A	N/A	N/A
Raster Conversion	Included – Optionally Instantiated						
Color Samples/Cycle	1	1	1	1 to 32	1	1	1 to 32
Number of LUTs in Xilinx FPGAs	3k	5k	6k	11k[1]	5k	6k	10k[1]
Available in RTL Source Code	✘	✘	✔	✔	✘	✔	✔
Available as targeted netlist	✔	✔	✔	✔	✔	✔	✔

1) Silicon Resources for two samples/cycle configuration, and 12 bits per color sample