# JPEG-E-T

## Tiny Baseline JPEG Encoder

XILINX

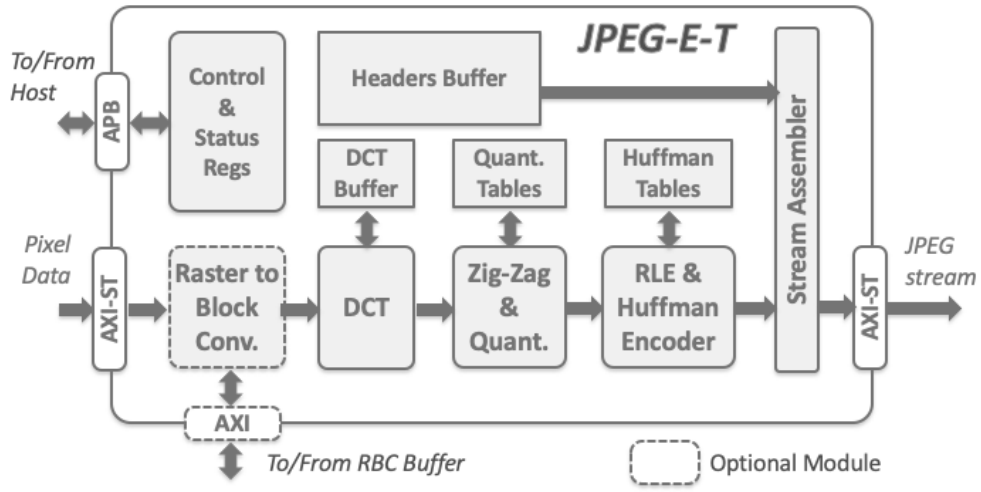
This JPEG compression IP core supports the Baseline Sequential DCT modes of the ISO/IEC 10918-1 standard. It implements an area-efficient, high-performance hardware JPEG encoder with remarkably low processing latency. Probably the smallest JPEG encoder IP core in the market, the JPEG-E-T occupies about 3,000 LUTs, 16 DSP and 3 BRAM when implemented on a Xilinx FPGA.

The encoder processes one color sample per clock cycle, enabling it to compress multiple Full-HD channels even in low-cost FPGAs. Once programmed, the easy-to-use encoder requires no assistance from a host processor to compress an arbitrary number of frames.

SoC integration is straightforward thanks to standardized AMBA® interfaces: AXI Streaming for pixel and compressed data, and a 32-bit APB slave interface for registers access. Users can optionally insert timestamps or other metadata in the compressed stream using a dedicated AXI Streaming interface.

The core is designed with industry best practices, and its reliability and low risk have been proven through both rigorous verification and customer production. Its deliverables include a complete verification environment and a bit-accurate software model.

## Block Diagram




## FEATURES

Extremely small JPEG encoder

### Standards Support

- ISO/IEC 10918-1 Standard Baseline Sequential DCT mode
- Encodes single-frame JPEG images and Motion JPEG payloads
- 8-bit per color samples
- Up to four color components; any image size up to 64k x 64k
- Handles all scan configurations and all JPEG formats
- APP, COM, and restart markers
- Programmable Quantization tables for image quality or bit-rate control

### Interfaces

- AXI Streaming I/O data interfaces
- APB Control/Status interface
- Optional AHB wrapper with DMA capabilities

### Performance and Size

- One encoded sample per clock cycle
- ~3,000 LUTs, 16 DSP, and 3 BRAM

### Ease of Integration

- Automatic program-once/encode-many operation
- Simple, dedicated timestamps interface
- Included bit-accurate software model generates test vectors, expected results, and core programming values
- Optional Raster-to-Block Conversion with AXI or standard memory interface to the lines buffer

### Format

- Available as a netlist for Xilinx FPGAs

## Applications

The JPEG-E-T core is suitable for systems supporting ultra-high frame resolutions and/or frame rates, such as: Corporate, airborne, and other security or surveillance systems, machine vision and video link decoders or terminals for industrial, or defense systems and medical imaging systems

## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The core has been verified through extensive synthesis, place and route, and simulation runs. It has been embedded in several shipping customer products and is proven in both ASIC and FPGA technologies.

## Silicon Resources Utilization

The JPEG-E-T core can be mapped to any Xilinx Device (provided sufficient silicon resources are available). The following table provides sample implementation and performance data for the default configuration of the core.

| Device Family | LUTs | DSPs | BRAMs | Freq (MHz) |
|---|---|---|---|---|
| Artix-7 (speed grade -1) | 2,622 | 16 | 2.5 | 166 |
| Kintex-7 (speed grade -1) | 2,612 | 16 | 2.5 | 200 |
| Spartan-7 (speed grade -2) | 2,617 | 16 | 2.5 | 130 |
| Kintex Ultrascale+ (speed grade -1) | 2,595 | 16 | 2 | 250 |
| Artix Ultrascale+ (speed grade -1) | 2,594 | 16 | 2 | 240 |
| Versal Prime (speed grade -2) | 2,492 | 16 | 2 | 250 |

Please note that these sample implementation figures do not represent the highest speed or smallest area possible for the core. Please contact CAST to discuss silicon resource utilization and performance for your target technology.

## Deliverables

The core is available as a targeted FPGA netlist and includes everything required for successful implementation. The deliverable package includes:

- Targeted FPGA netlist
- Sophisticated self-checking Testbench
- Software (C++) Bit-Accurate Model
- Sample simulation scripts
- Comprehensive user documentation

## JPEG Cores Available from CAST

This core is one member of the family of JPEG encoder and decoder cores that CAST offers. The following table summarizes the family members and indicates their basic features.

| JPEG IP Cores | **JPEG-E-T** Tiny Baseline JPEG Encoder | **JPEG-E-S** Baseline JPEG Encoder | **JPEG-EX-S** Extended JPEG Encoder | **JPEG-EX-F** Ultra-Fast Ext. JPEG Encoder | **JPEG-D-S** Baseline JPEG Decoder | **JPEG-DX-S** Extended JPEG Decoder | **JPEG-DX-F** Ultra-Fast Ext. JPEG Decoder |
|---|---|---|---|---|---|---|---|
| Functionality | Encoder | | | | Decoder | | |
| Baseline JPEG | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Extended Sequential JPEG | × | × | ✓ | ✓ | × | ✓ | ✓ |
| Motion JPEG Payload | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Sub-sampling Formats | Any with up to four components including Single–color, 4:4:4, 4:2:2, 4:2:0 | | | | | | |
| Image Resolution | 16x16 to 64k x 64k | | | | | | |
| Max. Sample Depth | 8 | 8 | 12 | 12 | 8 | 12 | 12 |
| Programmable Huffman Tables | × | ✓ | ✓ | ✓ | N/A | N/A | N/A |
| Rate Control | × | ✓ | ✓ | ✓ | N/A | N/A | N/A |
| Raster Conversion | Included – Optionally Instantiated | | | | | | |
| Color Samples/Cycle | 1 | 1 | 1 | 1 to 32 | 1 | 1 | 1 to 32 |
| Available in RTL Source Code | × | × | ✓ | ✓ | × | ✓ | ✓ |
| Available as targeted netlist | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |