JPEG-E-S

Baseline JPEG Encoder

This JPEG compression IP core supports the Baseline Sequential DCT modes of the ISO/IEC 10918-1 standard. It implements an area-efficient, high-performance, ASIC or FPGA, hardware JPEG encoder with remarkably low processing latency.

The JPEG-E-S encoder produces compressed JPEG images and the video payload for Motion-JPEG container formats. It accepts images with 8-bit color samples and up to four color components, in all widely-used color subsampling formats.

The encoder processes one color sample per clock cycle, enabling it to compress multiple Full-HD channels even in low-cost FPGAs. One of the smallest JPEG encoders available, it requires about 70,000 equivalent gates when mapped on an ASIC technology.

Once programmed, the easy-to-use encoder requires no assistance from a host processor to compress an arbitrary number of frames. SoC integration is straightforward thanks to standardized AMBA® interfaces: AXI Streaming for pixel and compressed data, and a 32-bit APB slave interface for registers access. Users can optionally insert timestamps or other metadata in the compressed stream using a dedicated AXI Streaming interface.

Customers with a short time to market priority can use CAST's IP Integration Services to receive complete JPEG subsystems. These integrate the JPEG encoder with video interface controllers, Hardware UDPIP or Transport Stream networking stacks, or other IP cores available from CAST.

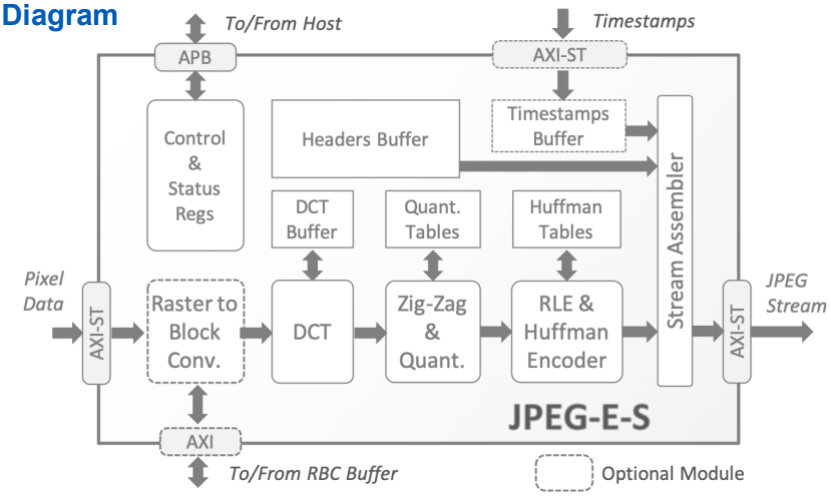
The core is designed with industry best practices, and its reliability and low risk have been proven through both rigorous verification and customer production. Its deliverables include a complete verification environment and a bit-accurate software model.

Applications

The JPEG-E-S core's low processing latency and ability to regulate compressed image size or video bit rate make it ideal for video streaming systems even in the presence of strict bandwidth and latency limitations. Suitable applications include:

- Consumer electronics or professional imaging products such as digital cameras, camcorders, and office automation equipment (printers, scanners, etc.).
- Residential, corporate, airborne, and other security or surveillance systems.
- Machine vision and video links for industrial, defense, or other systems.
- Medical imaging systems, and advanced driver assistance systems.

Block Diagram



FEATURES

Performs Baseline Sequential DCT JPEG encoding of images or video for ASICs or FPGAs, with small silicon area, high performance, and low latency.

Standards Support

- ISO/IEC 10918-1 Standard Baseline Sequential DCT mode
- Encodes single-frame JPEG images and Motion JPEG payloads
- 8-bit per color samples
- Up to four color components; any image size up to 64k x 64k
- Handles all scan configurations and all JPEG formats
- APP, COM, and restart markers
- Programmable Huffman and Quantization tables

Rate Control Options

- Image: Limits the size of each individual frame
- Video: Regulates bit rate over a number of input frames

Interfaces

- AXI Streaming I/O data interfaces
- APB Control/Status interface
- Optional AHB wrapper with DMA capabilities

Performance and Size

- One encoded sample per clock cycle
- Small silicon footprint (about 70k ASIC gates)

Ease of Integration

- Automatic program-once/encode-many operation
- Simple, dedicated timestamps interface
- Included bit-accurate software model generates test vectors, expected results, and core programming values
- Optional Raster-to-Block Conversion with AXI or standard memory interface to the lines buffer

Format

Available as a netlist for Intel FPGAs

www.cast-inc.com • info@cast-inc.com • tel +1 201.391.8300
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Silicon Resources Utilization

The JPEG-E-S core can be mapped to any Altera Device (provided sufficient silicon resources are available) and optimized to suit the particular project's requirements. The following table provides sample implementation and performance data for the default configuration of the core.

	1080p30 4:2:2	720p60 4:4:4	1080p60 4:2:2	Logic Resources	DSPs	Memory Bits
Max10	✓	×	×	9,300 LEs	8	48,540
CycloneV	✓	✓	×	3,443 ALMs	4	49,082
Arria10	✓	✓	✓	3, 443 ALMs	4	49,082

Note that the list of video formats is not exhaustive, and that these sample implementation figures do not represent the highest speed or smallest area possible for the core. Please contact CAST to discuss silicon resource utilization and performance for your target technology.

Verification

The core has been verified through extensive synthesis, place and route, and simulation runs. It has been embedded in several shipping customer products, and is proven in both ASIC and FPGA technologies.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available as a targeted netlist for ASIC and FPGA, and includes everything required for successful implementation. The deliverable package includes:

- Targeted FPGA netlist
- Sophisticated self-checking Testbench
- Software (C++) Bit-Accurate Model
- Sample simulation and synthesis scripts
- Comprehensive user documentation

JPEG Cores Available from CAST

This core is one member of the family of JPEG encoder and decoder cores that CAST offers. The following table summarizes the family members and indicates their basic features.

JPEG IP Cores	**JPEG-E-T** Tiny Baseline JPEG Encoder	**JPEG-E-S** Baseline JPEG Encoder	**JPEG-EX-S** Extended JPEG Encoder	**JPEG-EX-F** Ultra Fast Ext. JPEG Encoder	**JPEG-D-S** Baseline JPEG Decoder	**JPEG-DX-S** Extended JPEG Decoder	**JPEG-DX-F** Ultra Fast Ext. JPEG Decoder
Functionality	Encoder				Decoder		
Baseline JPEG	✓	✓	✓	✓	✓	✓	✓
Extended Sequential JPEG	×	×	✓	✓	×	✓	✓
Motion JPEG Payload	✓	✓	✓	✓	✓	✓	✓
Sub-sampling Formats	Any with up to four components including Single–color, 4:4:4, 4:2:2, 4:2:0						
Image Resolution	16x16 to 64k x 64k						
Max. Sample Depth	8	8	12	12	8	12	12
Programmable Huffman Tables	×	✓	✓	✓	N/A	N/A	N/A
Rate Control	×	✓	✓	✓	N/A	N/A	N/A
Raster Conversion	Included – Optionally Instantiated						
Color Samples/Cycle	1	1	1	1 to 32	1	1	1 to 32
Number of LUTs in Xilinx FPGAs	3k	5k	6k	11k[1]	5k	6k	10k[1]
Available in RTL Source Code	×	×	✓	✓	×	✓	✓
Available as targeted netlist	✓	✓	✓	✓	✓	✓	✓

1) Silicon Resources for two samples/cycle configuration, and 12 bits per color sample

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