JPEG-DX-F

Ultra-Fast Baseline and Extended JPEG Decoder

This JPEG decompression IP core supports the Baseline Sequential DCT and Extended Sequential DCT modes of the ISO/IEC 10918-1 standard. It implements a scalable, ultra-high-performance, ASIC or FPGA, hardware JPEG decoder that handles extremely high pixel rates.

The JPEG-DX-F Decoder decompresses JPEG images and the video payload for Motion-JPEG container formats. It accepts compressed streams of images with 8- or 12-bit color samples and up to four color components, in all widely-used color subsampling formats.

Depending on its configuration, the decoder processes from two to 32 color samples per clock cycle. Its high throughput capabilities are best exploited when decompressing streams produced by the JPEG-EX-F Encoder Core. This Encoder-Decoder pair provide an extremely cost-effective solution for streaming or archiving UHD (4K/8K) video, or very high frame rates at lower resolutions.

Once programmed, the easy-to-use decoder operates on a standalone basis, parsing marker segments and decompressing coded data with no assistance from a host processor. The decoder reports the image format (i.e., resolution, subsampling format, and color sample-depth) to the system, so that the decoded images are properly further processed and/or displayed.

SoC integration is straightforward thanks to standardized AMBA® interfaces: AXI Streaming for pixel and decompressed data, and a 32-bit APB slave interface for registers access.

Customers with a short time to market requirements can use CAST's IP Integration Services to receive complete JPEG subsystems. These integrate the JPEG encoder with video interface controllers, Hardware UDPIP or Transport Stream networking stacks, or other IP cores available from CAST.

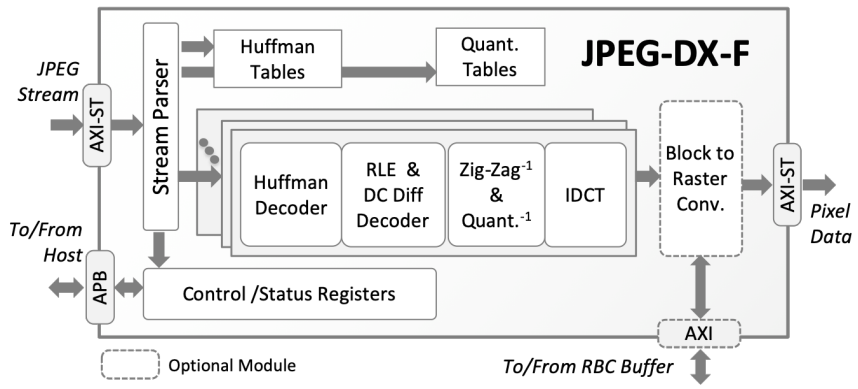
The core is designed with industry best practices, and its reliability and low risk have been proven through both rigorous verification and customer production. Its deliverables include a complete verification environment and a bit-accurate software model.

Applications

The JPEG-DX-F core's great throughput makes it suitable for systems supporting ultra-high frame resolutions and/or frame rates, such as:

- Corporate, airborne, and other security or surveillance systems.
- Machine vision and video link decoders/terminals for industrial or defense systems.
- Medical imaging systems.

Block Diagram



FEATURES

8/12-bit JPEG decoder for ASIC and FPGA with scalable, ultra-high performance

Standards Support

- ISO/IEC 10918-1 Standard Baseline and Extended Decoder (Sequential DCT modes)
- Single-frame JPEG images and Motion JPEG payloads
- Up to four color components
- 8- and 12-bit color samples
- All widely used color subsampling formats, and any image size up to 64k x 64k
- All scan configurations and all JPEG formats
- All marker segments except DNL
- Up to four Huffman Tables
- Up to four 8-bit or 18-bit Quantization tables

Interfaces

- AXI Streaming I/O data interfaces
- APB Control/Status interface
- Optional AHB wrapper with DMA capabilities

Performance

- Synthesis-time configurable scalable architecture
- Very high throughput: up to 32 samples per clock cycle
- Achieves maximum throughput when decoding streams produced by JPEG-EX-F

Ease of Integration

- Requires no programming or control from host
- Reports image format
- Detects and reports marker syntax errors
- Delivered with bit-accurate software model
- Optional Block-to-Raster Conversion with AXI or standard memory interface towards the lines buffer

Silicon Resources Utilization

The JPEG-DX-F can be mapped to any Lattice Device (provided sufficient silicon resources are available) and optimized to suit the particular project's requirements. The following table provides sample implementation and performance data for the core configured to process 2 samples per cycle (JPEG-DX-F/2) and under its default configuration.

Family / Device	Logic Resources	Memory Resources	Freq. (MHz)	MSamples/s
Igloo2 M2GL150-STD	16,269 4LUT	16 RAM64x18 3 RAM1K18	110	220
PolarFire MPF500T-STD	16,000 4LUT	27 uSRAM 2 LSRAM	150	300
RTG4 RT4G150 -STD	16,288 4LUT	16 RAM64x18 3 RAM1K18	80	160
SmartFusion2 M2S150-STD	16,269 4LUT	16 RAM64x18 3 RAM1K18	110	220

Note that the implementation figures do not represent the highest speed or smallest area possible for the core. Please contact CAST to discuss silicon resource utilization and performance for your target technology.

Verification

The core has been verified through extensive synthesis, place and route and simulation runs. It has also been embedded in several products, and is proven in both ASIC and FPGA technologies.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available in source code RTL (Verilog) or as an FPGA netlist, and its deliverables include everything required for successful implementation:

- Sophisticated self-checking Testbench
- Software (C++) Bit-Accurate Model
- Sample simulation and synthesis scripts
- Comprehensive user documentation

JPEG Cores Available from CAST

This core is one member of the family of JPEG encoder and decoder cores that CAST offers. The following table summarizes the family members and indicates their basic features.

JPEG IP Cores	**JPEG-E-T** Tiny Baseline JPEG Encoder	**JPEG-E-S** Baseline JPEG Encoder	**JPEG-EX-S** Extended JPEG Encoder	**JPEG-EX-F** Ultra Fast Ext. JPEG Encoder	**JPEG-D-S** Baseline JPEG Decoder	**JPEG-DX-S** Extended JPEG Decoder	**JPEG-DX-F** Ultra Fast Ext. JPEG Decoder
Functionality	Encoder				Decoder		
Baseline JPEG	✓	✓	✓	✓	✓	✓	✓
Extended Sequential JPEG	✗	✗	✓	✓	✗	✓	✓
Motion JPEG Payload	✓	✓	✓	✓	✓	✓	✓
Sub-sampling Formats	Any with up to four components including Single–color, 4:4:4, 4:2:2, 4:2:0						
Image Resolution	16x16 to 64k x 64k						
Max. Sample Depth	8	8	12	12	8	12	12
Programmable Huffman Tables	✗	✓	✓	✓	N/A	N/A	N/A
Rate Control	✗	✓	✓	✓	N/A	N/A	N/A
Raster Conversion	Included – Optionally Instantiated						
Color Samples/Cycle	1	1	1	1 to 32	1	1	1 to 32
Available in RTL Source Code	✗	✗	✓	✓	✗	✓	✓
Available as targeted netlist	✓	✓	✓	✓	✓	✓	✓

1) Silicon Resources for two samples/cycle configuration, and 12 bits per color sample