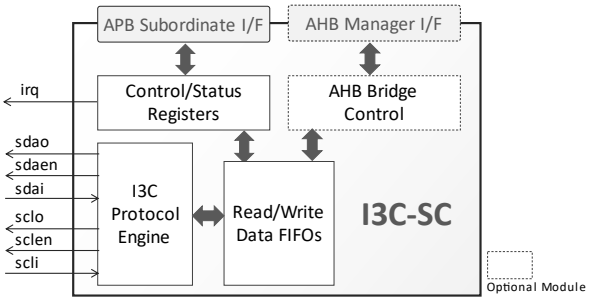
I3C-SC

MIPI I3C Basic Secondary Controller

The I3C-SC core implements a versatile MIPI® Improved Inter Integrated Circuit (I3C) Secondary Controller core compliant with the latest MIPI I3C Basic℠ specification.

As a secondary controller, the I3C-SC can act either as a bus target or a bus controller. Compliant to the I3C Basic specification, the core communicates in Single Data Rate (SDR) mode but can tolerate High Data Rate (HDR) traffic. It can coexist and communicate with legacy I2C devices, and it can optionally be configured to operate as such in an I3C or I2C bus.



When acting as a target, the I3C-SC needs no firmware support to parse and execute the broadcast or direct Common Command Codes (CCCs) relevant to I3C Basic targets. It can be assigned a Dynamic Address by the bus controller or use its legacy I2C static address, it supports Hot-Join and can generate In-Band Interrupts when directed by the host to do so. When the I3C-SC core is the only bus controller, then Hot-Join is not possible, and static addressing should be used.

Designed for easy integration, the I3C-SC can operate in two different modes. Under *normal mode*, data from private I3C or legacy I2C write transfers are stored to a FIFO and made available to the host via an APB Subordinate interface. In a similar way, the host provides data to be used for private I3C or legacy I2C read transfers via the core's APB subordinate interface. Alternatively, the core can operate in I3C-to-AHB *bridging mode*, where it autonomously converts private I3C or legacy I2C transfers to accesses on its AHB manager port using a simple yet configurable over-I3C protocol. Under the I3C-to-AHB bridging mode, the core acts as a an I3C bus target, needs no software assistance, and provides the I3C bus controller access to the local AHB bus, enabling remote monitoring, configuration, debug, or data exchange. The selection between normal and bridging operation modes is under software control via the core's control register.

The highly flexible core offers synthesis-time and run-time configuration options, which allow adapting its size and behavior to the application requirements. For example, the AHB-manager interface and the clock domains synchronizers can be removed at synthesis to reduce the core's silicon footprint. During run-time, the I3C private data and I2C traffic can be bridged to the core's AHB-manager interface or transferred to and from the host via the core's APB subordinate interface. Also, parameters defining the CCCs processing (e.g. own-static-address, provisional ID), the over-I3C protocol (e.g. number address bytes, max number of data bytes) and the AHB-manager port behavior (e.g., AHB burst type & address wrapping) are all run-time configurable via the core's registers.

The I3C-SC core adheres to the industry's best coding and verification practices to ensure trouble-free implementation in ASIC or FPGA technologies. Technology mapping, constraining, and scan insertion are straightforward, as the core contains no multi-cycle or false paths and uses only rising-edge-triggered D-type flip-flops, no tri-states, an asynchronous reset line per clock domain, and clean clock domain crossing modules. Its reliability and low risk have been proven through rigorous verification and FPGA validation

FEATURES

I3C Features

- I3C Basic Secondary Controller
- Up to 12.5 Mbit/s, SDR-Capable and HDR-Tolerant
- Autonomous processing of Broadcast and Direct Common Command Codes (CCCs) relevant to an I3C Basic target
- Hot-Join Mechanism
- In-Band Interrupts
- I3C Bus and Device Characteristic Registers (BCR & DCR)
- Dynamic Addressing Assignment participation in the Target mode
- Optional operation as a legacy I2C device, and interoperable with legacy I2C devices
  - Supports I2C static addressing, I2C messaging, and a 50ns spike filter

Easy to Use & Integrate

- Run-time selectable operation modes:
  - Autonomous I3C-to-AHB bridge
  - Firmware-assisted, I3C controller or target exchanging data with the host via APB-accessible registers or implementing a custom over-I3C protocol
- Standardized AMBA interfaces
  - APB-Subordinate for register access
  - AHB-Manager (when I3C-to-AHB bridging mode is enabled)
- Independent clocks for APB. AHB and I2C with clean clock domain crossing
- Fully synchronous, scan-ready, LINT-clean design

Configuration Options

- Synthesis-Time: FIFO sizes, AHB-manager Interface and Clock Synchronizers instantiation, maximum number of I3C bus targets
- Run-Time: Data traffic source & target selection (AHB-manager I/F or APB Accessible Registers & FIFOs), and FIFO

Applications

The I3C-SC core can add economical and low-power I3C data transfer capabilities to sensors, actuators, power regulators, analog front-ends, microcontroller peripheral devices, microcontrollers, or even FPGA devices and designs.

Implementation Results

The I3C-SC can be mapped to any Intel FPGA device. The following table provides sample FPGA resources utilization data. Please contact CAST to get characterization data for your target configuration and technology.

Device	Configuration	Logic Resources (ALMs)	Clock Frequency (MHz)
Cyclone 10 (speed grade 6)	Small: No AHB Mgr, no CDC, 16x8 FIFOs, 4 I3C devices	1,928	61
	Large: AHB Mgr, CDC, 32x8 FIFOs, 8 I3C devices	2,839	59
Arria 10 GX (speed grade 1)	Small: No AHB Mgr, no CDC, 16x8 FIFOs, 4 I3C devices	1,933	76
	Large: AHB Mgr, CDC, 32x8 FIFOs, 8 I3C devices	2,826	74
Agilex (speed grade 1)	Small: No AHB Mgr, no CDC, 16x8 FIFOs, 4 I3C devices	1,963	89
	Large: AHB Mgr, CDC, 32x8 FIFOs, 8 I3C devices	3,306	87

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been rigorously verified through extensive synthesis, place and route, simulation runs, with in-house and 3rd party verification. The core is silicon-proven.

Deliverables

The core is available in synthesizable RTL and FPGA netlist forms. It ships with everything required for successful implementation, including:

- Verilog RTL source code
- Post-synthesis EDIF (netlist licenses)
- Testbenches for behavioral and post-synthesis verification
- Simulation & Synthesis scripts
- Documentation

About the MIPI I3C Basic Specification

The MIPI I3C Basic specification is a subset of the MIPI I3C Specification that is publicly accessible and intended to be implementable by non-MIPI organizations under a RAND-Z license.

The Royalty-free MIPI I3C Basic provisions a multidrop two-wire serial bus operating up to 12.5MHz that provides many of the I3C protocol innovations, including in-band interrupts, dynamic address assignment and backward compatibility with I2C.

Learn more at MIPI I3C official web page.