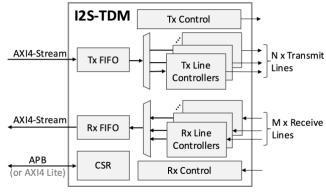# I2S-TDM

I2S/TDM Audio Transceiver

intel FPGA

The I2S-TDM IP core is a highly configurable, full-duplex, multichannel serial audio transceiver. The transceiver can act as a controller (master) or a target (slave) for Inter-IC Sound (I2S) and Time-Division Multiplexed (TDM) audio interfaces, exchanging multi-channel audio samples over a configurable number of serial lines (pins).

The I2S-TDM offers a number of configuration options to satisfy a wide range of serial audio interface requirements. The operation mode (controller or target), sample width, sample rate, frame format, number of channels and their allocation to physical lines are all programmable at run time. At synthesis time, designers can choose the maximum number of audio channels and serial data lines the transceiver can support.

The core is designed for ease of use and integration and adheres to the industry's best coding and verification practices. The core's control and status registers (CSR) are accessed through a 32-bit AMBA® APB interface, or, optionally, an AXI4 Lite interface. The host system exchanges audio data with the core either via this CSR interface or via dedicated AXI4-Stream interfaces. The system interfaces operate with a clock that is independent from the audio master and serial bit clocks, and the core implements clean clock domain crossing boundaries.

The I2S-TDM core is available in Verilog source code or as a targeted FPGA netlist. Its deliverables include a testbench, comprehensive documentation, sample simulation and synthesis scripts, and bare-metal device drivers.

Size and Performance

The I2S-TDM core can be mapped in any Intel FPGA device. The FPGA silicon resources required for its implementations depend on the core configuration. The following are sample implementation data for the core configured to support 1 transmit line, 1 receive line, and 8 audio channels per direction.

Family	Logic Resources	Memory Resources	Freq. (MHz)
Cyclone® 10 (-i5)	832 ALM	2 RAMB	100
Arria®10 GX (-i3)	831 ALM	2 RAMB	143
Agilex™ 7 (-e2v)	1068 ALM	2 RAMB	125

These results do not represent the smallest possible area requirements nor the highest possible clock frequency. Please contact CAST to get accurate characterization data for your target application and core configuration.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available

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