I2S-TDM

I2S/TDM Audio Transceiver

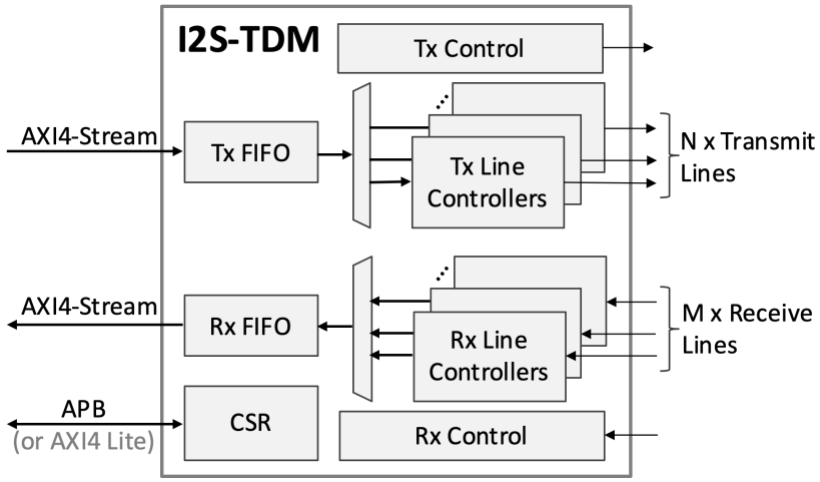
The I2S-TDM IP core is a highly configurable, full-duplex, multichannel serial audio transceiver. The transceiver can act as a controller (master) or a target (slave) for Inter-IC Sound (I2S) and Time-Division Multiplexed (TDM) audio interfaces, exchanging multi-channel audio samples over a configurable number of serial lines (pins).

The I2S-TDM offers a number of configuration options to satisfy a wide range of serial audio interface requirements. The operation mode (controller or target), sample width, sample rate, frame format, number of channels and their allocation to physical lines are all programmable at run time. At synthesis time, designers can choose the maximum number of audio channels and serial data lines the transceiver can support.

The core is designed for ease of use and integration and adheres to the industry's best coding and verification practices. The core's control and status registers (CSR) are accessed through a 32-bit AMBA® APB interface, or, optionally, an AXI4 Lite interface. The host system exchanges audio data with the core either via this CSR interface or via dedicated AXI4-Stream interfaces. The system interfaces operate with a clock that is independent from the audio master and serial bit clocks, and the core implements clean clock domain crossing boundaries.

The I2S-TDM core is available in Verilog source code or as a targeted FPGA netlist. Its deliverables include a testbench, comprehensive documentation, sample simulation and synthesis scripts, and bare-metal device drivers.

Block Diagram



FEATURES

Serial Audio Transceiver

- Left-justified and right-justified I2S and TDM audio data formats
- Full-duplex operation
- Configurable number of receive and transmit data lines (pins), and number of audio channels

Software-Controlled Parameters per Direction (Tx and Rx)

- Controller (master) or target (slave) mode of operation
- Sample width of 2 to 32 bits
- Sample rate (bit clock period and polarity)
- Frame format (Fsync/WS duration, delay and polarity)
- Implemented serial data lines and the number of channels per line

Synthesis Time Configuration Options

- Number of transmit and receive serial data lines
- Maximum number of transmit and receive audio channels
- Receive and transmit FIFO size

SoC System Interfaces

- 32-bit AMBA APB or AXI4 Lite for control and status register access
- Audio data input/output via register interface, or via dedicated 32-bit AXI-Stream interfaces
- Maskable interrupts based on programmable FIFO occupancy thresholds

Deliverables

- LINT-clean Verilog RTL source code or targeted FPGA netlist
- Integration testbench
- Simulation & synthesis scripts
- Comprehensive user documentation
- Bare-metal device drivers
- FPGA evaluation boards available on request

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available

Size and Performance

The silicon resources required for the implementation of the I2S-TDM IP core depend on its configuration. A configuration with one transmit line, one receive line, and eight audio channels per direction requires about 10,000 gates, when FIFOs are implemented as flops. The host and audio master clocks can run at frequencies exceeding 1GHz in modern ASIC technologies. Please contact CAST to get accurate characterization data for your target configuration and technology.