H264-OIP-HDD

H.264 Video Over IP – HD Decoder Subsystem

This Video Over IP Subsystem integrates H.264 Decompression, Transport Stream and RTP/UDP/IP decapsulation to enable the rapid development of complete video streaming products. Hardware reference designs and customization services complete the solution.

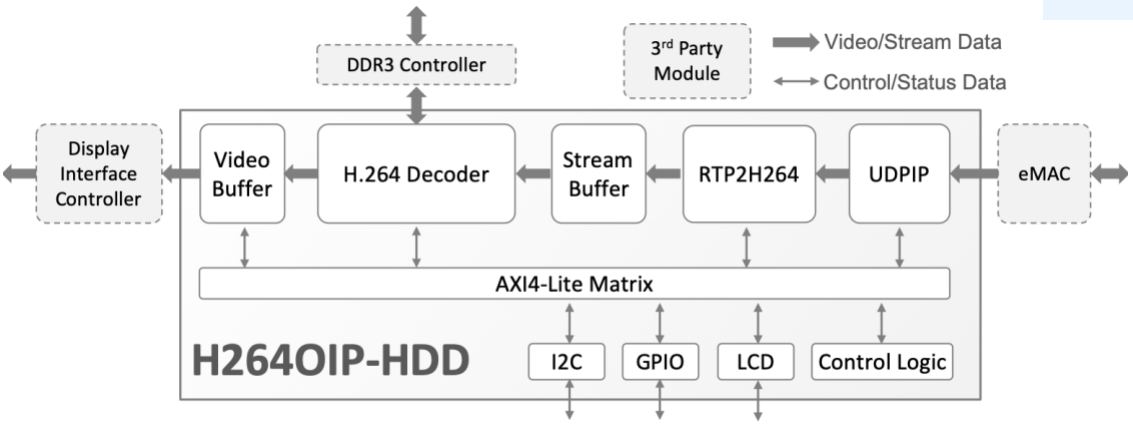
The subsystem uses the Low-Latency AVC/H.264 Baseline Profile Decoder Core and the RTP and UDPIP, hardware stacks available from CAST. Flexible interfaces allow easy integration of video, memory, and network controllers, and AXI4-Lite slave interfaces allow a host processor to access all control and status registers. An optional custom logic module allows standalone, processor-free operation and provides access to control and status registers via UDP packets. Video and stream data are transferred among the subsystem's modules using AXI-Stream, making removing or adding modules straightforward.

The subsystem can decode Constrained Baseline Profile streams, encapsulated in RTP or plain UDP and features, sub-frame latency (no frame buffers are implemented).

Applications

The H264OIP-HDD Subsystem is suitable for broadcasting, surveillance, industrial, defense, and medical live-streaming applications. The software-free platform consumes significantly less energy than software based solutions, making it ideal as a decompression coprocessor in battery-operated devices with video streaming capabilities.

Block Diagram



FEATURES

- Ultra-Low Latency H.264 Video Decompression
  - Constraint Baseline Profile
  - RTP and UDPIP Decapsulation
  - Sub-frame latency capable
- Host interface via AXi4-Lite or processor-free UDP-controlled operation
- AXI4-ST bus for Video & Stream data
- Supports HD – 720p30/60 and Full-HD – 1080p30

Customization Options

- Integration with Video-Out Controllers (e.g., DVI, HDMI, MIPI-CSI, or SDI)
- Integration with IP-based MAC controllers (e.g., Ethernet or 802.11 WiFi)

Reference FPGA Designs

- Drive display via HDMI, on Xilinx or Intel boards
- Can work with CAST's H.264 Encoder Subsystem Reference Designs

Reference Designs

A turnkey reference design for Xilinx and Intel FPGA development boards (see Table below) is readily available. The reference design integrates the H264OIP-HDD-HDE Subsystem with Xilinx's or Intel's Ethernet MAC core. The reference design can be ported to other FPGA boards up on request.

FPGA Family and Platform	Video-Out	Stream In	3rd Party Cores	Video Formats
Xilinx Kintex-7, KC705	HDMI	1G Ethernet	Xilinx TEMAC and DDR3 controller LogiCores	720p30/60, 1080p@30
Intel Arria 10 / DK-DEV-10AX115S-A	HDMI	1G Ethernet	Intel eMAC controller	720p30/60, 1080p@30
Intel Arria V / DK-START-5AGXB3N	HDMI	1G Ethernet	Intel eMAC controller	720p30/60, 1080p@30

Customization Services

CAST can integrate the H264OIP-HDD subsystem with your choice of video-out, memory, and network controllers. We can also modify it to support different CAST decompression cores.

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