

H16750S

UART with FIFOs, IrDA and Synchronous CPU Interface

The H16750S is a standard UART providing 100% software compatibility with the popular Texas Instruments 16750 device. It performs serial-to-parallel conversion on data originating from modems or other serial devices, and performs parallel-to-serial conversion on data from a CPU to these devices.

The H16750S can be run in either 16450-compatible character mode or FIFO mode, where an internal FIFO relieves the CPU of excessive software overhead. An IrDA-compliant serial data port may be used for infrared communication.

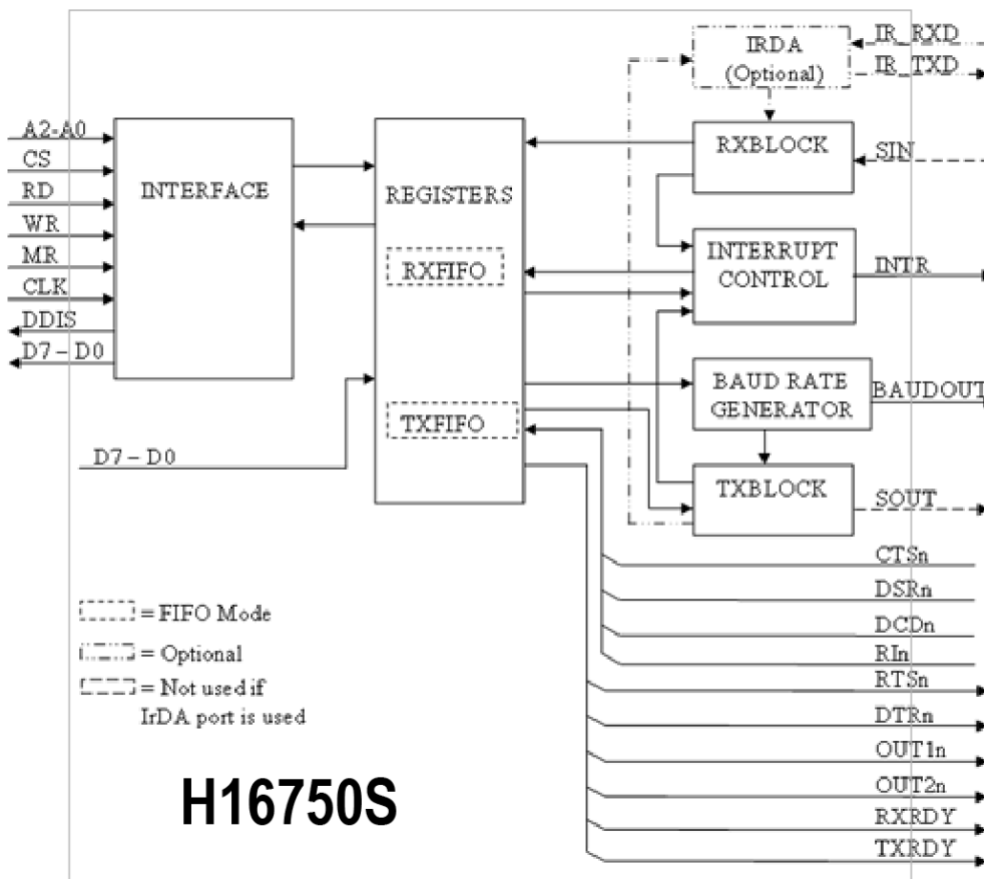
Developed for easy reuse in FPGA or ASIC applications, the H16750S is available optimized for several technologies with competitive utilization and performance characteristics.

Applications

The H16750S can be utilized for a variety of serial communication applications including:

- Serial or modem computer interface
- Serial interface within modems and other devices

Block Diagram



FEATURES

- Capable of running all existing 16450 and 16550a software
- Fully Synchronous design. All inputs and outputs are based on rising edge of clock
- In FIFO mode, the transmitter and receiver are each buffered with 16 byte FIFOs to reduce the number of interrupts presented to the CPU
- Available with FIFO sizes of 8, 16, 32, 64, 128 or 256 bytes
- Adds or deletes standard asynchronous communication bits (start, stop and parity) to or from the serial data
- Independently controlled transmit, receive, line status and data set interrupts
- Programmable baud generator divides any input clock by 1 to $(2^{16} - 1)$ and generates the 16 x clock
- Modem control functions (CTS_n, RTS_n, DSR_n, DTR_n, RIn and DCD_n)
- Programmable Auto-CTS_n and Auto-RTS_n
- In Auto-CTS_n mode, CTS_n controls the transmitter
- In Auto-RTS_n mode, the receiver FIFO contents and threshold control RTS_n
- Serial Port has an optional Infrared Data Association (IrDA) data port
- Fully programmable serial interface characteristics:
 - 5, 6, 7, or 8 bit characters
 - Even, odd, or no-parity bit generation and detection
 - 1, 1½, or 2 stop bit generation
 - Baud generation
- False start bit detection
- Complete status register
- Line break generation and detection
- Internal diagnostic capabilities: loopback controls for communications link fault isolation
- Full prioritized interrupt system controls
- Optional IrDA or AMBA™ APB or CoreConnect™ OCP Bus Interface

Functional Description

The H16750S includes the following major blocks. All the core's inputs and outputs are fully synchronous to the rising edge of the CLK input.

Interface (Read/Write Control Logic)

Handles communication with the processor (or parallel) side of the system. Manages all writing and reading of internal registers.

UART Registers

Holds all of the device's internal registers. Some information comes from the other blocks, however register information is gathered in the UART Registers block and made available to all blocks.

Receiver Block

Handles the receiving of the incoming serial word. It is programmable to recognize data widths such as 5, 6, 7 or 8 bits, various parity settings, and different stop bits of 1, 1½ and 2 bits. It checks for errors in the input data stream, and if the incoming word has no problems it is placed either in the Receiver Holding register or in the Receiver FIFO depending on the mode programmed.

Interrupt Control

Sends an interrupt signal back to the processor depending on the state of the FIFO and its received and transmitted data. Various levels of interrupt can be read from the Interrupt Identification register. Interrupts are sent in the condition of empty transmission or receiving buffers (or FIFOs), an error in receiving of a character, or other conditions requiring the attention of the processor.

Baud Rate Generator

Takes the input clock, CLK, and divides it by a programmed value (from 1 to $2^{16} - 1$). This divided clock is then divided by 16 to create the transmission clock called the Baudout clock.

Transmit Block

Handles the transmission of data written to the Transmission Holding register (or transmit FIFO). It adds required start, parity and stop bits to the data being transmitted so that the receiving device can do the proper error handling and receiving.

IrDA (Optional)

The IrDA block is an optional addition to the H16750S. It handles the same data as the SIN and SOUT only in an Infra Red Interface format.

Component Substitution

The H16750S core is modeled after the Texas Instruments 16750. Check with CAST for a list of differences from the original device.

Implementation Results

H16750S reference designs have been evaluated in a variety of technologies. The following are sample results excluding the FIFOs:

ASIC Technology	Approx. Area	Frequency (MHz)
TSMC 40 nm	4670 gates	300
TSMC 28 nm	3781 gates	300
TSMC 16 nm	4001 gates	300

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive synthesis, place and route, and simulation runs. It has been embedded in several shipping customer products, and is proven in both ASIC and FPGA technologies.

Deliverables

The core is available in synthesizable RTL and FPGA netlist forms, and includes everything required for successful implementation, including a sophisticated self-checking testbench, simulation scripts, test vectors, and expected results, synthesis scripts and comprehensive user documentation.