

EMAC-1G

Gigabit Ethernet Media Access Controller

Implements an Ethernet Media Access Controller compatible with the 10/100 Mbps IEEE 802.3 and 1Gbps IEEE 802.3-2002 specifications. The controller provides half- or full-duplex operation, supports jumbo frames, and optionally provides a useful set of statistics counters enabling station management.

A host processor can control the operation of the core via a slave interface that provides access to its control and status registers. The EMAC-1G features two master ports for data transfers, one for transmit and one for receive. The two DMA engines use buffer descriptors to automatically transfer data from local FIFOs to an external shared memory. The core supports 32-bit AMBA/AHB or Wishbone SoC buses; other bus interfaces are available on request.

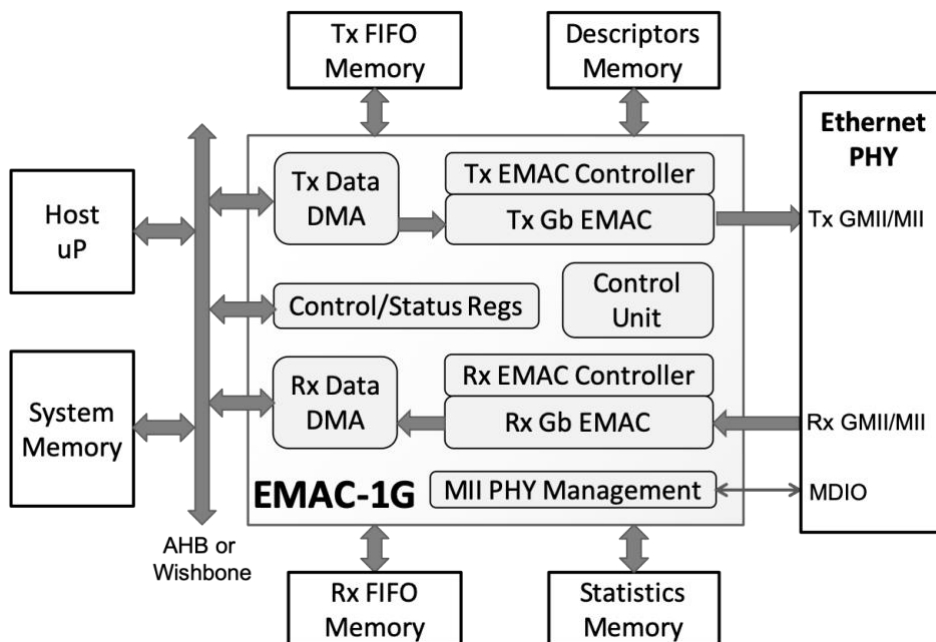
Integration with an Ethernet PHY is straightforward, as the controller core supports the Media Independent Interface (MII) and the Gigabit Media Independent Interface (GMII) physical layer interface standards.

The EMAC-1G is production proven in ASIC and FPGA technologies.

Applications

The EMAC-1G can be used in any SoC design requiring Ethernet connectivity.

Block Diagram



FEATURES

Data Link Layer

- Programmable 10/100 or 1000 Mbps operation
- IEEE 802.3-2002 specification with preamble, start-of-frame delimiter (SFD), and CRC generation and checking
- Full- or half-duplex operation
- CSMA/CD procedures for half duplex
- Flow control for full duplex
- Jumbo frames
- Flexible address filtering
- Extensive statistics counters
- Detection of too long or too short packets, with programmable length limits

PHY Interfaces

- Media Independent Interface (MII) for 10/100Mbps
- Gigabit Media Independent Interface (GMII) for 1Gbps
- MDIO interface for PHY configuration and management
- Optional Reduced Media Independent Interface (RMII)
- Optional Reduced Gigabit Media Independent Interface (RGMII)
- Optional Serial Gigabit Media Independent Interface (SGMII)

Host Interface

- AMBA/AHB or Wishbone 32-bit slave for status and control
- One interrupt line per Tx and Rx.
- Clock switch control port (10/100 or 1000 Mbps)

DMA controller

- AMBA/AHB or Wishbone 32-bit master separate for Tx and Rx
- Big or little endian data byte ordering
- Scatter/Gather capabilities
- Configurable number of Buffer-Descriptors

Transmit/Receive dual port Synchronization RAMs

- Operate as internal configurable FIFOs with programmable threshold levels
- Configurable sizes up to 16kB

Implementation Results

The provided figures do not represent the higher speed or smaller area for the core. Area, power and speed depend on configuration, optimizations, process, and libraries. Contact CAST to get characterization data for your target configuration and technology.

Technology	Frequency (MHz)	Eq. NAND2 Gates
TSMC 40nm G	25	28,352
	50	28,352
	125	28,354
TSMC 65nm LP	25	29,013
	50	29,013
	125	29,027
TSMC 65nm GP	25	27,068
	50	27,068
	125	27,069
TSMC 90nm G	25	25,015
	50	25,017
	125	25,024
SMIC 130nm	25	24,853
	50	24,872
	125	25,412

Verification

The core has been verified through extensive synthesis, place and route, and simulation runs. It has been embedded in several shipping customer products, and is proven in both ASIC and FPGA technologies.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available in Verilog RTL or as targeted FPGA netlist, and its deliverables include everything required for a successful implementation, including an extensive testbench, comprehensive documentation and a sample Linux driver.