DMA Controllers IP Cores Family

Memory-to-memory, streaming, multichannel, and scatter-gather cores for diverse data movement

DMA Controllers	DMA-CTRL	AXI4-DMA	MC-SDMA	AXI4-SGDMA
Memory-to-Memory	Yes	No	Yes (Stream IFs Loopback)	Yes (with two cores)
Memory-to/from-Stream	No	Yes	Yes	Yes
Number of stream I/F	N/A	2	Up to 32	1
Descriptor Lists	Single Descriptor on CSRs	Linear List (Queue) on CSRs	Single Descriptor per Stream Interface on CSRs	Linear or Cyclic, Linked or Incremental Scatterlists in Memory / Single Descriptor on CSRs
Bus Bridging	AHB ⇔ AHB, AXI ⇔ AXI, AHB ⇔ AXI	AXI4 ⇔ AXI4-Stream	AXI4 ⇔ AXI4-Stream AXI4 ⇔ AXI4	AXI4 ⇔ AXI4-Stream AXI4 ⇔ AXI4
Width Conversion & CDC	No	With external AXI4-Stream bridge	With external AXI4-Stream bridge	Yes
Data Width	Configurable	32 or 64 bits	32-512 bits	32–512 bits
Burst Size	Fixed	Programmable	Programmable	Programmable
Unaligned Accesses	No	No	No	Yes
Peripheral-Triggered Transfers	Yes	No	Yes	Yes
Split Transfers with Stride	No	No	Yes	No
Availability	Now	Now	Now	Now
Verification Environment	Verilog	System Verilog	UVM	System Verilog