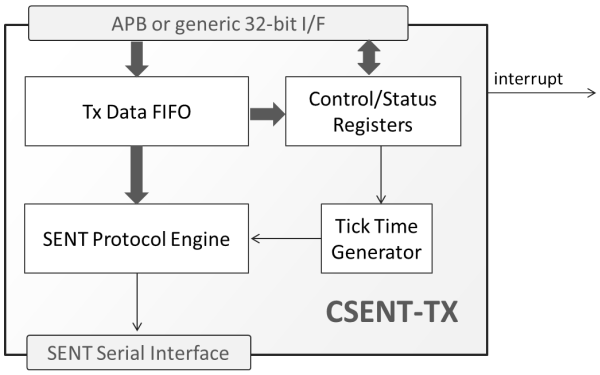
CSENT-TX

Enhanced SENT/SAE J2716 TX Controller

The CSENT-TX core implements a transmitter for the Single Edge Nibble Transmission (SENT) protocol. It complies with the SAE J2716 standard and supports both synchronous and asynchronous transmission modes.

Under asynchronous mode, the core autonomously, without requiring any extra action from the host system, initiates transmission, as soon as data become available in its input-data register. Under synchronous mode, transmission is triggered by either the host system via the core's control registers, or when the core receives a valid master trigger pulse via the SENT interface.



Designed for ease of use and integration, the core reports its status using two signals, one indicating that a transmission is in progress, and a second one reporting the completion of a frame's transmission. Furthermore, the CSENT-TX provides access to its control, status, and data registers via a 32-bit APB, or an AXI4 or a generic subordinate interface. Implementation of the core is straightforward, as the core contains no latches or tri-states, is fully synchronous with a single clock domain, and includes no multicycle or false paths.

The CSENT-TX core is designed with industry best practices, has been rigorously verified and is production proven.

Size and Performance

The core can be mapped to any ASIC technology and any FPGA device. The following are sample implementation results, which do not represent the highest speed or smallest area possible for the core and exclude the FIFOs.

Target Technology	Core Configuration	Logic Resources	Memory Resources	Freq
Agilex 5 *A5EA013BB23BE5S*	No FIFO Asynchronous Transmitter only	79 ALMs	-	625 MHz
Cyclone 10GX *10CX220YF672I5G*		64 ALMs	-	625 MHz
Agilex 5 *A5EA013BB23BE5S*	Sensor's Trigger Pulse Protocol Mode 8 x 32-bit FIFO Synchronous and Asynchronous Transmitter	326 ALMs	256 bits	350 MHz
Cyclone 10GX *10CX220YF672I5G*		307 ALMs	256 bits	400 MHz

Applications

The CSENT-TX core is suitable for automotive microcontrollers and SoCs.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

FEATURES

SENT/SAE J2716 Transmitter

- Fast Channel and Slow Channel
- 4-bit CRC checking for Fast Channel and Slow Short Serial Message
- 6-bit CRC checking for Slow Enhanced Serial Message
- Option to include Status Nibble in the CRC checksum
- Short (8-bit data) and Enhanced (12- or 16-bit data) Message Formats for Slow Channel
- Asynchronous / Synchronous mode transmitter
- Sensor's Trigger Pulse (STP) protocol mode
- Automatic data rate synchronization
- Selectable data length (1 to 6 nibbles) and Pause pulse option
- Supports inverted SENT protocol

Ease of Integration

- 32-bit APB, AXI4, or generic subordinate interface
- Optional Transmit FIFO of configurable size
- Run-time programmable configuration registers
- Synthesis-time defined reset values for all registers, enables data autonomous transmitting
- LINT-clean, single-clock domain, scan-ready design

Deliverables

- RTL source code or targeted FPGA netlist
- SystemVerilog Testbench
- Sample synthesis and simulation scripts
- Documentation
- IP XACT Register Definitions