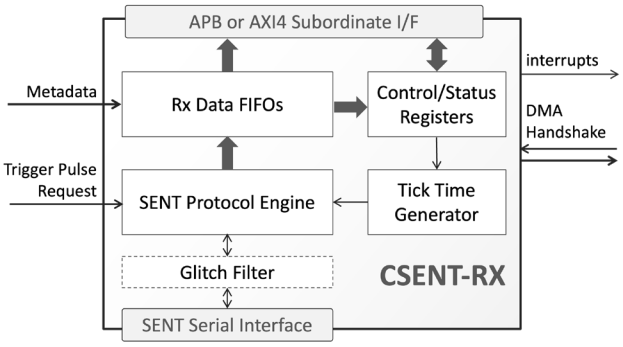
CSENT-RX

Enhanced SENT/SAE J2716 RX Controller

altera™
An Intel Company

The CSENT-RX core implements a receiver for the Single Edge Nibble Transmission (SENT) protocol. It complies with the SAE J2716 standard and supports both synchronous and asynchronous sensors. It can be used for receiving data from one or multiple sensors using a single SENT line.



The CSENT-RX provides access to its control, status, and data registers via a 32-bit APB, or AXI4-Lite bus interface, and the reset values for all its control registers are defined at synthesis time.

The core provides a glitch filter on the serial data input and has data mapping functionality on received data to offload the connected host from data formatting. An external metadata port allows the host system to add customized metadata (e.g. timestamps) into the received data stream. The received data are accessible via the register interface. The core is also capable of generating trigger pulses requesting synchronous sensors to send data. The generation of trigger pulses is controlled via a dedicated input pin, or via a control register. A set of handshaking signals facilitates the integration with an external DMA controller. An extended set of interrupt sources includes detection of calibration variation, timeout errors, frequency drift error, FIFO-related triggers, frames' validity and numerous frame's errors.

The CSENT-RX core is designed with industry best practice, has been rigorously verified and is production proven.

Size and Performance

The CSENT-RX core can be mapped to any Altera FPGA device provided sufficient resources are available. The following are sample implementation results, which do not represent the highest speed or smallest area possible for the core and exclude the data FIFOs.

Target Technology	Core Configuration	Logic Resources	Freq
Agilex 5 *A5EA013BB23BE5S*	No data mapping No metadata CRC4 only No synchronous Trigger Pulse Frame No Timeout functionality	621 ALMs	275 MHz
Arria 5GX 5AGXBB3D4F35C5		696 ALMs	175 MHz
Cyclone 10GX 10CX220YF672I5G		620 ALMs	275 MHz
Agilex 5 A5EA013BB23BE5S	Data mapping and Metadata CRC4, CRC 6 and CRC8 Synchronous Trigger Pulse Frame Timeout functionality	933 ALMs	275 MHz
Arria 5GX 5AGXBB3D4F35C5		901 ALMs	150 MHz
Cyclone 10GX 10CX220YF672I5G		906 ALMs	275 MHz

Applications

The CSENT-RX core is suitable for automotive microcontrollers and SoCs.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

FEATURES

SENT/SAE J2716 Receiver

- Fast and Slow Channel
- 4,6 or 8-bit CRC checking
- Programmable Glitch filter
- All types of SENT Frames
  - Programmable data length (1 to 8 nibbles) for Fast Channel Frames
  - Short (8-bit data) and Enhanced (12- or 16-bit data) Message Formats for Slow Channel
- Fast Channel data mapping to reduce host/CPU overhead
- Customized metadata support
- Supports inverted SENT protocol

Trigger Pulse for Synchronous Sensors

- Allows up to four sensors (transmitters) to use the same physical SENT connection
- Programmable trigger pulse length
- Activated via software or hardware

Ease of Integration

- 32-bit APB or AXI4-Lite interface, and comprehensive set of interrupts
- Programmable reference counter to validate calibration pulses
- Optional Receive FIFO of configurable size for Fast Channel data
- Run-time programmable configuration registers
- Synthesis-time defined reset values for all registers, enables data reception without control from host processor
- LINT-clean, single-clock domain, scan-ready design

Deliverables

- RTL source code or targeted FPGA netlist
- SystemVerilog testbench
- Sample synthesis and simulation scripts
- Documentation
- IP XACT register definitions

CAST

www.cast-inc.com • info@cast-inc.com