CAN-CTRL

CAN 2.0, CAN FD, & CAN XL Bus Controller

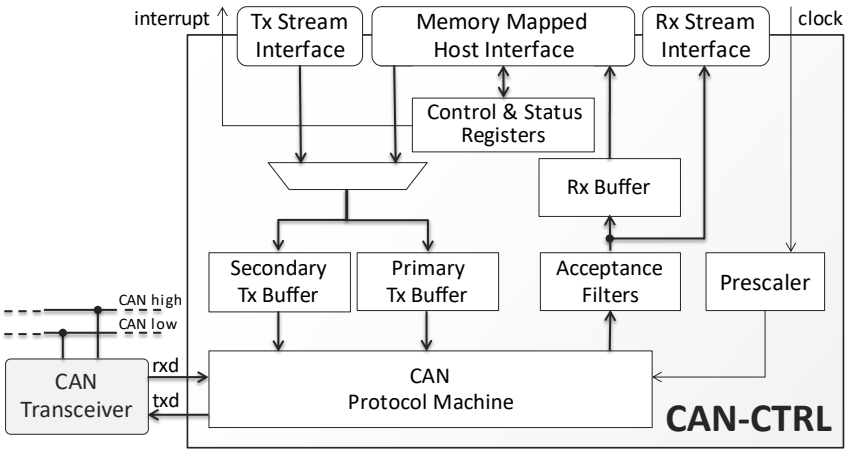
The CAN-CTRL implements a highly featured and reliable CAN bus controller that performs serial communication according to the Controller Area Network (CAN) protocol. It supports classical CAN and CAN FD according to ISO 11898-1:2015; CAN XL as specified in CiA 610-1 specification; Time-Triggered CAN (TTCAN) per ISO 11898-4; and CAN Frame time-stamping as described in the CiA 603 profile. This CAN controller core handles data rates exceeding 20Mbit/s and it is optimized for the AUTOSAR and SAE J1939 specifications.

The CAN-CTRL is especially efficient in minimizing host CPU overhead and simplifying software development. It automatically drops incoming messages using run-time programmable acceptance filters, so that unwanted messages never reach the host system. The core also enables flexible scheduling of outgoing messages with minimum software overhead. To this end, the core implements two transmit buffers: the primary transmit buffer (PTB) and the secondary transmit buffer (STB). The PTB is able to store one CAN frame while the number of stored frames inside the STB is configurable. The STB may operate either in FIFO mode or may do frame reordering based on the priority of the CAN frame ID. The PTB has always highest priority regardless of the frame ID. Furthermore, polling the status of the core is not necessary because an interrupt line—driven by runtime maskable sources—notifies the host about actionable events on the CAN data bus or in the CAN controller core.

Designed for ease of integration, the CAN-CTRL is controlled by and exchanges data with the host system via a single memory-mapped slave interface. This memory-mapped interface can be either a generic 32-bit or 8-bit parallel interface, or optionally a 32-bit AMBA® APB, AHB-Lite, Wishbone, or Avalon-MM interface. Data can optionally be transferred to and from the core via dedicated 32-bit Avalon ST streaming interfaces. Using these dedicated streaming interfaces might be preferable in cases where messages are transferred to and from the system memory by an external DMA engine or when tight integration with a CANsec or other custom-hardware engine is required. To avoid limiting the host system, the host interfaces operate in an independent clock domain, which can be either synchronous or asynchronous to the core clock. Finally, to ease network operation, the core implements functionality similar to the Philips SJA1000 working with its PeliCAN mode extensions, providing error detection and analysis, bus diagnostics and optimization features.

Proven in hundreds of shipping products, certified by reputable testing houses, verified with third-party VIP, conformance-tested in plugfests, and developed to CAST's stringent quality standards, the CAN-CTRL is likely the most reliable CAN controller IP core available.

Block Diagram



FEATURES

CAN Specifications Support

- Classical CAN & CAN-FD (ISO 11898-1:2015, & legacy versions)
- CAN XL (CiA 610-1 specification)
- TTCAN (ISO 11898-4 level 1)
- CAN Frame time-stamping (CiA 603)
- Optimized for AUTOSAR and SAE J1939

Enhanced Functionality

- Error Analysis features enabling diagnostics, system maintenance, and system optimization: Last error type, Arbitration lost position, and Error Warning Limit
- Listen-Only Mode enables CAN bus traffic analysis and automatic bit-rate detection
- Loopback mode for self-testing

Flexible Message Buffering and Filtering

- Configurable number of:
  - Receive and transmit buffers
  - Independently programmable acceptance filters
- FIFO or priority mode for transmit frames, and high-priority transmit buffer for urgent traffic

Easy to Use and Integrate

- Programmable data rate; the data rate is practically limited by the transceiver and/or the bus configuration
- Programmable baud rate prescaler
- Single-Shot Transmission Mode for lower software overhead and fast reloading of transmit buffer
- Programmable interrupt sources
- Data access via a memory-mapped interface or via dedicated streaming interfaces
- Compatible with any ISO 11898-2 and CAN SIC (CiA 601-4) transceiver

Safety Enhanced Version (optional)

- ISO-26262 ASIL-D Ready
- Implements ECC for SRAM and spatial redundancy for inner logic protection

Highly Reliable

- Proven in hundreds of automotive, aerospace, and industrial products
- Certified by testing houses, as part of customer products
- Robustly verified using internal test suite, and 3rd party VIPs
- Plugfest-tested

Variants and Versions

The CAN bus controller comes in three variants: 2.0, FD, and XL. The 2.0 variant supports only the CAN 2.0 specification, the FD variant adds support for CAN FD, and the XL variant supports the CAN 2.0, CAN FD, and CAN XL standards.

Each of the three core variants is available in two versions: Standard, and Safety-Enhanced. The Safety-Enhanced version implements ECC for SRAMs protection and uses spatial redundancy for protecting the inner logic of the core. The Safety-Enhanced versions are certified as *ISO-26262 ASIL-D Ready*.

Applications

The CAN-CTRL core can be integrated in devices that use CAN or higher-layer, CAN-based communication protocols. In addition to traditional automotive applications, such devices are used in industrial (e.g., CANopen and DeviceNet protocols), aviation (e,g., ARINC-825 and CAN aerospace protocols), marine (e.g., NMEA 2000 protocol) and other applications.

Implementation Results

CAN-CTRL can be mapped to any ASIC technology or FPGA device (provided sufficient silicon resources are available). The following are sample results for the core configured with three receive buffers, three transmit buffers, and three acceptance filters (does not include priority mode, TTCAN and CiA603 timestamping).

Configuration	Technology	Cell Area (eq. Gates)	Memory Bits
CAN 2.0	TSMC 28nm HPC	9,000	2,688
CAN FD	TSMC 28nm HPC	11,000	6,272
CAN XL	TSMC 28nm HPC	15,000	133,248
CAN 2.0 – Safe	TSMC 28nm HPC	30,000	3,864
CAN FD – Safe	TSMC 28nm HPC	35,000	9,212
CAN XL – Safe	TSMC 28nm HPC	45,000	216,528

Please contact CAST to get characterization data for your target configuration and technology.

Verification

The core has been rigorously verified through extensive synthesis, place and route, simulation runs, Verification IP, and plugfests. It has been embedded in numerous shipping customer products and is proven in both ASIC and FPGA technologies. Several customer products have been certified for compliance by independent testing houses.

Support & Maintenance

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

The core will be modified if needed, to remain compatible with future versions of CiA's specification and with future updates of the related ISO 11898-1 standard. Customers shall receive updates for as long as they remain under support and maintenance coverage.

Deliverables

The core is available in synthesizable RTL and FPGA netlist forms. It ships with everything required for successful implementation, including:

- VHDL or Verilog RTL source code, or targeted FPGA netlist
- Testbenches for behavioral, and post-synthesis verification
- Simulation and Synthesis scripts
- Low-Level Hardware Abstraction Layer (HAL) and Linux driver
- Optional MISRA C non-OS, bare-metal driver with advanced software examples
- User Documentation and RUVM register descriptions.

The optional safety-enhanced package further includes the Safety Manual (SAM), a Failure Modes, Effects and Diagnostics Analysis (FMEDA) and the ASIL-D Ready certificate, issued by SGS-TÜV Saar GmbH.