CAMFE

Camera Front-End Processor

The CAMFE Core implements a flexible, resource-efficient camera front-end processor that receives raw pixel data from a CMOS or CCD sensor and outputs a video stream ready for display, further processing, or compression.

The core first converts the Bayer pattern output from the sensor to an RGB image using an efficient de-mosaicing interpolation filter. The interpolated RGB samples are input to the White Balancing stage, which adjusts color intensities so they are appropriate for reproduction in a display. Under its full configuration, the core subsequently proceeds with further steps essential for optimizing the visual quality of the image, running RGB to YUV color space conversion, then performing Contrast Stretching (also called Normalization) and Gamma Correction, and finally applying a Sharpening Filter.

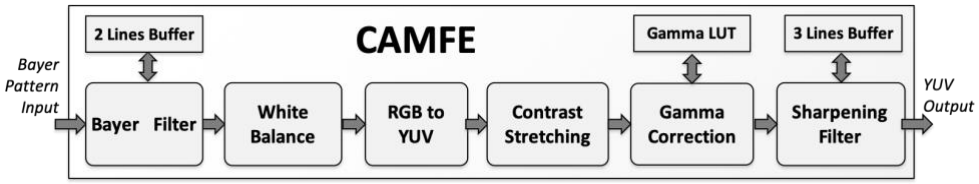
The CAMFE Core requires only a few lines of buffering and adds minimal processing latency. It features extremely low power consumption due to the absence of a power-consuming frame buffer and the core's small silicon footprint (less than 15,000 gates). Furthermore, a fine-pipelined structure allows CAMFE to operate at high clock frequencies, and it can process over 150 Mpixels/sec even in low-end FPGAs.

The core is designed with industry best practices, and its reliability and low risk have been proven through both rigorous verification and customer production. Its deliverables include a complete verification environment and a bit-accurate software model.

Applications

The CAMFE is suitable for interfacing a CMOS or CCD sensor in a variety of applications that display, process or compress images such as medical imaging, surveillance, autonomous or unmanned vehicles, biometrics analysis, and video streaming,

Block Diagram



Size and Performance

The following are sample implementation results, not representing the highest speed or smallest area that may be achieved.

Target Technology	Area	Performance
TSMC 28nm (hpm-sc9-svt-c31)	6,386 µm2	5000 MPixels/sec
Xilinx, Artix-7	780 LUTs	200 MPixels/sec
Altera, Stratix V	590 ALMs	200 MPixels/sec

FEATURES

CMOS or CCD sensor interface, delivering quality-optimized RGB or YUV images ready for display, compression or further processing

Processing Pipeline

- Bayer Interpolation/De-mosaicing
- RGB to YUV Conversion
- Visual Quality Enhancements
  - White Balancing
  - Contrast Stretching (Normalization)
  - Gamma Correction
  - Sharpening Filter

Low-Power with Low Latency

- Minimal buffering for low-latency and low-power operation
  - Only five lines of buffering under its full configuration (two for Bayer filtering, and three for image sharpening)
- Optimized, small implementation requires less than 15,000 equivalent gates

Performance

- Fine pipeline allows processing up to over 150 Mpixels/sec even in low-end silicon

Input / Output Formats

- 10bit/sample Raster-Scan Bayer Input, 8bit/Sample-Raster-Scan YUV Output
- Up to two Mpixels, optionally extendable for higher resolution

Maturity

- Robustly verified and production proven

Deliverables

- Source code VHDL or Verilog RTL or targeted netlist
- Testbench and Bit-Accurate C-Model
- Sample synthesis and simulation scripts

Sourced from ocean logic