CACHE-CTRL

AHB Cache Controller

The CACHE-CTRL IP core is a flexible cache memory controller providing a 32-bit slave processor interface and a 32-bit master interface to the memory subsystem. The processor and memory interfaces are natively AHB5 and can easily be reduced to AHB-lite.

The cache controller core supports a four-way associative cache memory and implements a Least Recently Used (LRU) replacement policy. The number of cache lines and the cache line width are configurable at synthesis time. The core only caches read accesses and invalidates the cached data if a write access to a cached memory location occurs.

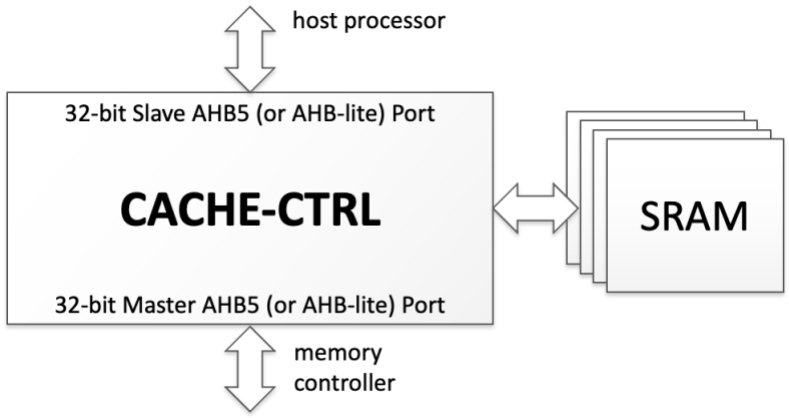
Mapping the cache controller to any Xilinx® FPGA is straightforward, as the core does not require any device-specific cells or SRAM modules; it used only using standard, single-ported SRAMs that are easily mapped to block RAM. Integration of the core is trouble-free, as the core uses standard 32-bit AHB interfaces and supports clock gating.

The CACHE-CTRL core has been robustly verified and is silicon-proven.

Applications

The CACHE-CTRL can be used to add single or multilevel cache memory to cache-less deeply embedded processors, DSPs, or ASIPs. This can decrease the read access time and bandwidth to a relatively slow or energy consuming memory resource like flash, EEPROM, or DRAM devices. For example, it allows embedded processors like the BA2x, or the RISC-V BA51, or ARM's Cortex-M to run code directly from an off-chip NOR-flash (XIP) while minimizing the typical performance and/or power penalties of off-chip access.

Block Diagram



Implementation Results

The CACHE-CTRL core can be mapped to any Xilinx® FPGA. When configured with eight words per line and 256 lines per set (or 1024 lines in total) it synthesizes to about 2,000 LUTs and can run with over 100MHz in most 7-Series devices. Please contact CAST to get resource utilization and performance information for your preferred core configuration and FPGA devices.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Customization

The core interfaces and the cache's parameters (e.g., associativity, or replacement policy) can be customized. Please contact CAST to discuss your project requirements.

FEATURES

Adds single or multilevel cache memory to originally cache-less deeply embedded processors, DSPs, or ASIPs. Improves access time and reduces bandwidth to DRAM, Flash or EEPROM memories; enables XIP without typical power or performance penalties.

Cache Parameters

- Four-way set associative cache
- Least Recently Used (LRU) replacement policy
- Synthesis-time configurable:
  - number of cache lines
  - number of words per line
- 32-bit words
- Invalidates cache contents if a write access occurs

Easy Integration & Implementation

- AHB5 of AHB-lite interfaces
  - 32-bit slave port towards the processor
  - 32-bit master port towards the memory system
- Uses four single-ported SRAMs: no special type of RAM is required
- Scan-ready design
- Supports clock gating

Deliverables

- Verilog RTL source code or targeted FPGA netlist
- Verification environment using System Verilog Assertions and Bus Functional Models
- Sample synthesis and simulation scripts
- User Documentation