BA51

Low-Power Deeply Embedded RISC-V Processor

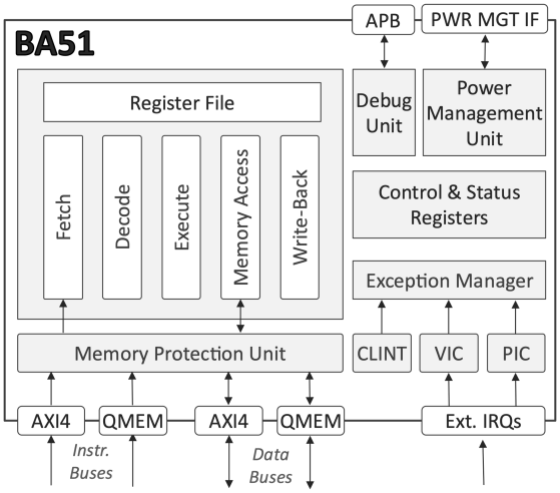
The BA51 is a highly configurable, low-power deeply embedded RISC-V processor IP core. It implements a single-issue, in-order, 2-stage execution pipeline, supporting the RISC-V 32-bit base integer instruction set (RV32I), or the 32-bit base embedded instructions set (RV32E).

Configuration Options for Broad Application Support

The processor core can be configured to meet different application requirements. It can optionally support user and supervisor privilege modes, as well as the ISA extensions for Compressed Instructions (C), Integer Multiplication and /Division instructions (M), Atomic Instructions (A), User-Level Interrupts (N), Control and Status Register (Zicsr), and Instruction-Fence (Zifencei). Support for the single-precision floating-point (F) ISA extension can also be added upon request.

Furthermore, the BA51 supports software and timer interrupts and up to 64 external interrupt lines. It features a remarkably low interrupt response time, which makes the core ideal for real time control applications. The time elapsed from when an external interrupt is asserted until the first instruction in the resolved interrupt handler can be issued is just 4 clock cycles.

The user can minimize the core's silicon footprint by choosing not to implement internal modules such as the machine mode internal timers and counters; the vectored interrupt controller (VIC); or the debug, power management (PMU), or memory protection (MPU) units. Finer-grained controls give customers the means to further tune the processor's features and size to their specific design needs, including the number and size of memory regions for the MPU, the mapping of memory addresses to interfaces, and the width of the instruction and data buses.



Compact & Energy Efficient

Designed for low power the BA51 is compact and enables advanced power management. Under its minimal configuration the processor size is just 16k gates, and even when most of the optional features are enabled, its size is in the order of 50k gates. This small silicon footprint is critical for minimizing leakage currents during idle or standby modes and for reducing dynamic power consumption. The BA51 also enables dynamic clock gating or power shut-off of unused modules, and also software or hardware controller dynamic frequency scaling of the bus and the CPU.

Furthermore, delivering more processing power per MHz than most processors in its class, the BA51 can be configured to operate at low frequencies to further save power, or to meet the most demanding embedded processing requirements, or any optimum combination of both.

Easy Integration and Low Risk

The processor core uses AMBA™, AXI-4 and low-latency Quick-access Memory (QMEM) interfaces for fetching instructions and accessing data and peripherals, while the debug unit connects to an external JTAG/TAP controller via an APB port.

Part of the family of processor cores available from CAST for nearly ten years and used by hundreds of customers, the BA51 IP core has been designed for easy reuse and integration, has been rigorously verified, and is LINT-clean, scan-ready and silicon proven. It is available in Verilog source code for ASICs or targeted netlists for FPGAs.

FEATURES

Low-Power Embedded Processor

- Small silicon footprint for lower leakage and dynamic CPU power
  - From 2.8 sq. µm in 16nm, or approximately 16k gates
- Advanced power management
  - Dynamic clock gating and power shut off of unused units
  - Software- and hardware-controlled clock frequency
- Single-issue, in-order, 2-stage pipeline
- Harvard architecture with separate instruction and data AXI- Lite and Quick-access Memory (QMEM) buses

Performance

- 3.0 Coremarks/MHz
- Over 500 MHz in 16 nm

RISC-V Features

- 32-bit Base RISC-V ISA (I/E) with optional M, A, Zicsr, Zifencei, C, and N Extensions
- F ISA extension upon request
- Supervisor, User, and Machine Modes
- Memory protection unit with configurable number of regions
- Core Local Interrupt Controller (CLINT) for timer and software interrupts
- Programmable and/or Vectored Interrupt Controller (PIC or VIC) for up to 64 direct external interrupts

Available Pre-Integrated Platforms

- Integrate bus fabric with peripherals such as GPIO, UART, Real-Time Clock, Timers, I2C, and SPI
- Optionally customized to include memory controllers, interconnects and more from the CAST IP line

Deliverables

- Available in Verilog source-code or as targeted FPGA netlist
- Comprehensive Documentation
- Testbench and sample simulation scripts

Sourced from BEYOND SEMICONDUCTOR

Applications

The royalty-free, energy-efficient BA51 processor can be employed as an effective replacement for existing 8-bit and 16-bit microcontrollers, or used as secondary, housekeeping or peripheral controller processor in complex SoC designs. It is suitable for a wide range of deeply embedded applications such as mixed-signal embedded processing (e.g. SERDES control), wireless communications ICs (e.g. Bluetooth, Zigbee, or GPS), and industrial microcontrollers.

Support and Services

The core as delivered is warranted against defects for 90 days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

IP Integration Services are also available to help minimize time to market for BA51-based systems. The processor core can be delivered pre-integrated with bus infrastructure cores, typical microcontroller peripherals, memory controllers, and interconnect IP cores. Contact CAST Sales for details.

Deliverables

The core is available for ASICs in synthesizable Verilog source code or for FPGAs in optimized netlists. It includes everything required for successful implementation: extensive documentation, a testbench, a sample SoC design, and sample synthesis and simulation script.

Reference designs on FPGA boards are also available; contact CAST Sales for information.