BA22-DE

32-bit Deeply Embedded Processor

XILINX

The royalty free BA22-DE is a compact yet powerful 32-bit processor for deeply embedded applications. It is a Harvard-style processor able to run at relatively high clock frequencies (more than 800MHz in 28nm), with a surprisingly small silicon footprint (base version is just 15K gates). Highly configurable to allow a variety of size/performance trade-offs, the BA22-DE can be used as a microcontroller in numerous applications, including mixed signal processing, portable and wireless devices, and automotive systems.

The BA22-DE uses separate instruction and data buses, and it has a pipeline depth of 4 or 5 stages depending on its configuration. The processor connects to the system via AMBA® AHB™, AXI4™, or Wishbone interfaces. It is also equipped with dedicated Quick Memory (QMEM) interfaces to tightly-coupled memories—which offer fast and deterministic access to code and data—and can be used for inter-core communication in a multi-core architecture.

Its base version includes 16 to 32 general-purpose registers (GPRs), a tick timer (TTimer), a programmable interrupt controller (PIC), an advanced power management unit (PMU), and optionally a debug unit (DBGU). The core's processing capabilities can be enhanced further with the optional hardware multiplier (MUL), divider (DIV), Multiply-Accumulate (MAC), IEEE 754 compliant floating point, and DSP instructions acceleration units. Its interrupt response time can also be optimized with the addition of a Vectored Interrupt controller (VIC).

The BA22-DE supports the variable instruction length BA2 instruction set, benefits from its extreme code density, and is binary compatible with other members of the BA2x processor family. Programming is facilitated with the included C/C++ toolchain, BeyondStudio™ Eclipse-based IDE, architectural simulator, and ported C libraries. Advanced debugging capabilities and off-the-shelf development boards can further ease software development.

Additional microcontroller peripherals may be ordered for pre-integration and delivery with the core, individually or in a complete platform. IP Integration Services are also available to help integrate any BA22 processor configuration with memory controllers, image compression, or other CAST IP cores.

Part of the royalty-free BA2x family, the BA22-DE processor core has been designed for easy reuse and integration, has been rigorously verified, and is production proven.

Block Diagram
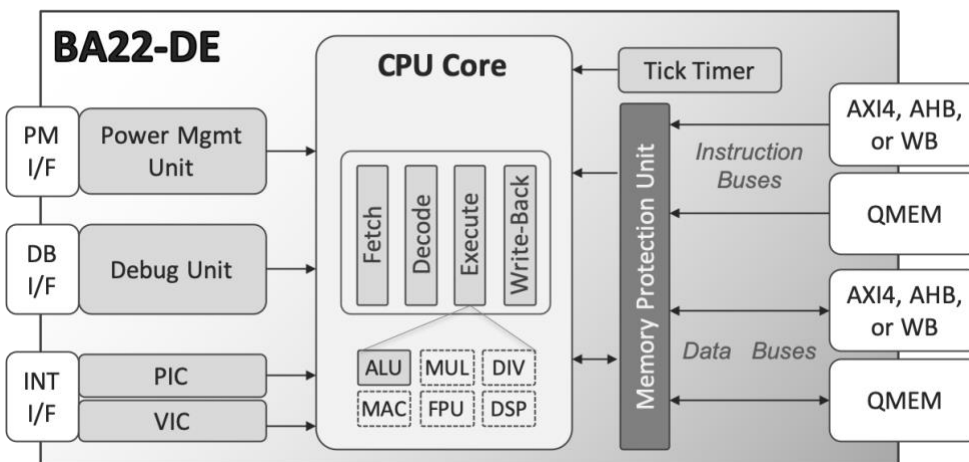
FEATURES

High Performance 32-bit CPU
- 2.93 CoreMarks/MHz
- Single-cycle execution on most instructions
- Fast interrupt response
- Optional hardware multiply, divide, multiply accumulate, DSP instructions acceleration, and floating point units.

Low Power Consumption
- Industry-leading code density minimizes instruction memory area & power
- Small silicon footprint (from 11,000 sq. um in 28 nm technology, or 15K eq. gates) consumes less leakage energy

Flexible Memory Access
- Tightly-coupled Quick Memory for fast and deterministic code and/or data access
- Instruction and/or data memories can also be connected to the AHB, AXI4 or Wishbone bus
- Optional Memory Protection Unit

Efficient Power Management
- Dynamic clock gating and power shut-off of unused units
- Software- and hardware-controlled clock frequency
- Wake-up on tick timer or external interrupt

Advanced Debug Capability
- Non-intrusive debug/trace for both CPU and system
- Complex chained watchpoint and breakpoint conditions
- Standard JTAG and proprietary Two-Wire Debug interfaces

Integrated Peripherals
- Base configuration includes a 32 bit-wide tick timer and a programmable interrupt controller
- Optionally pre-integrated with AMBA bus infrastructure, Vectored interrupt controller, DMAs, GPIOs, UARTS, Timers, SPI, I2C, memory controller and other IP cores from CAST

Easy Software Development
- Beyond Studio IDE for Windows, Linux
- ANSI C/C++ compiler, debugger, linker, assembler, & utilities
- Architectural simulator
- Ported libraries & RTOS

Ready for Evaluation
- Talos-BA2x Evaluation Kit includes a debug key, FPGA board with reference design, drivers and software

The BA2 Instruction Set

The BA2 instruction set provides extreme code density without compromising performance, ease of use, or scalability. It features:

- A linear, 32-bit address space
- Variable length instructions: 16, 24, 32, or 48 bits
- Simple memory addressing modes
- 12 to 32 general purpose registers
- Efficient flow-control, arithmetic, and load/store instructions
- Floating point and DSP extensions

Software Development

The core is delivered with BeyondStudio™, a complete Integrated Development Environment (IDE) for Windows and Linux under Eclipse. BeyondStudio includes a highly featured source code editor, supports graphical source-level debugging and GUI based configuration, and can be extended with a collection of available or custom plug ins.

The IDE integrates an Instruction level simulator and a GNU cross-compiling toolchain. The GNU Compiler Collection (GCC), includes front ends for C, C++, Objective-C, Fortran, Java, and Ada; libraries for these languages (e.g. libstdc++, libgcj, etc) are provided. The toolchain also includes the GNU Binutils collection of binary tools, and the GNU Project Debugger (GDB).

Extensive support of libraries enables easy application development for Linux and Android. Finally, hardware targets can be interfaced with the cost effective Beyond Debug Key, which in addition to standard JTAG (IEEE 1149.1 and IEEE 1149.7) also supports proprietary One Wire Debug and Two Wire Debug protocols.

Support and Services

The core as delivered is warranted against defects for 90 days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

IP Integration Services are also available to help minimize time to market for BA22-based systems. The processor core can be delivered pre-integrated with bus infrastructure cores, typical microcontroller peripherals, memory controllers, and interconnect IP cores. Contact CAST Sales for details.

Implementation Results

The following results reported from Xilinx tools, assume a 4kx64 RAM connected to the IQEM bus, an 8kx32 RAM connected to the DQEM bus, that all clocks are driven by a common source, and that all core I/Os are routed off-chip.

Family Device	Area (slices)	BRAM*	Clock (MHz)	Tools Version
Spartan-6 XC6SLX150T-3	1,267	32	72	ISE 13.4
Virtex-5 XC5VLX110-3	1,359	16	104	ISE 13.4
Virtex-6 XC6SLX130T-3	1,367	16	120	ISE 13.4

* Memory required for the implementation of QMEMs, not he CPU

The provided figures do not represent the higher speed or smaller area for the core. Area, power and speed depend on core configuration and tool optimizations. Furthermore power consumption depends on power management, software and memories configuration. For accurate characterization on your application please contact CAST.

Deliverables

The core is available for Xilinx FPGAs in optimized netlists. It includes everything required for successful implementation: extensive documentation, a testbench, a sample SoC design, sample synthesis and simulation scripts, and the BeyondStudio™ Eclipse-based software development IDE for Windows and Linux.

Reference designs on FPGA boards are also available; contact CAST Sales for information.

Related Products

The BA2x™ Processor Family includes a set of royalty-free, pre-configured products intended for different applications:

- **BA20 PipelineZero 32-bit Embedded Processor**, an ultra-low power processor using zero pipeline stages for instruction execution to provide maximum energy and performance efficiency.
- **BA21 32-bit Low-Power Deeply Embedded Processor**, a dual-pipeline low-power processor that delivers better performance than most processors its size.
- **BA22-CE 32-bit Cache-Enabled Embedded Processor**, a 4- or 5-stage pipelined processor, with instruction and data caches.
- **BA22-AP Basic Application Processor**, a 5-stage pipelined, cache- and MMU-enabled processor.
- **BA25 Application Processor**, a 7/12-stage pipelined, out of order, cache- and MMU-enabled processor.