BA22-AP

32-bit Basic Processor

The royalty free BA22-AP is a 32-bit processor for demanding embedded applications that use off-chip instruction and data memories and that may need to run a real-time operating system (RTOS) or a full operating system such as Linux or Android. Part of the royalty-free BA22 family, this processor core is extremely competitive in terms of high performance and low power consumption and has best-in-class code density.

The core has Instruction and Data Memory Management Units (MMUs) and Caches, optional dedicated buses for tightly coupled on-chip Instruction and Data memories, and an AMBA® AHB™, AXI-4™ or Wishbone system bus interface.

Its base version includes 32 general-purpose registers (GPRs), a tick-timer (TTimer), a programmable interrupt controller (PIC), an advanced power management unit (PMU), and optionally a debug unit (DBGU). The core's processing capabilities can be enhanced further with the optional hardware Multiply-Accumulate (MAC), IEEE 754 compliant floating-point, and DSP instructions acceleration units. Its interrupt response time can also be optimized with the addition of a Vectored Interrupt controller (VIC).

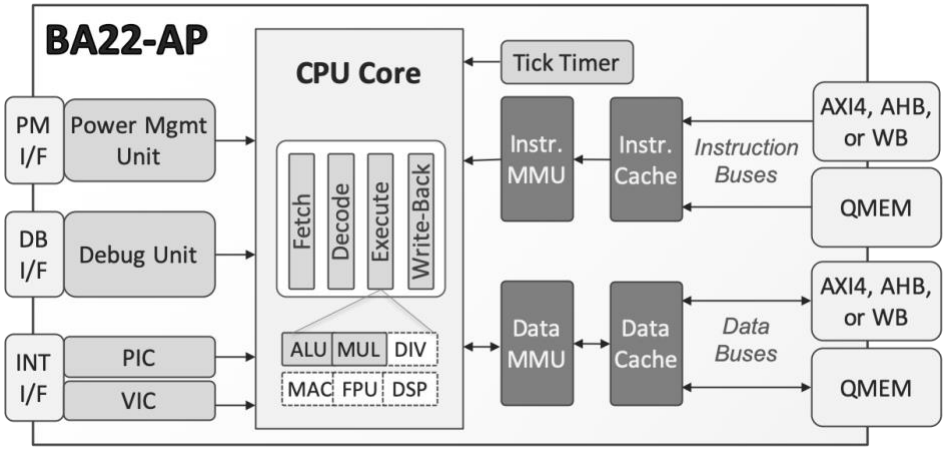
The BA22-AP supports the variable instruction length BA2 instruction set, benefits from its extreme code density, and is binary compatible with other members of the BA2x processor family. Programing is facilitated with the included C/C++ tool chain, Eclipse IDE, architectural simulator, and ported C libraries. Advanced debugging capabilities and off-the-shelf development boards can further ease software development.

In a typical 28 nm technology, the BA22-AP synthesizes to 38,000 sq. um (or 55k gates, excluding Cache and MMU RAMs) and can be clocked at up to 1000 MHz. Performance is rated at 2.93 Coremarks/MHz.

Additional microcontroller peripherals may be ordered for pre-integration and delivery with the core, individually or in a complete platform. IP Integration Services are also available to help integrate any BA22 processor configuration with memory controllers, image compression, or other CAST IP cores.

Part of the royalty-free BA2x family, the BA22-AP processor core has been designed for easy reuse and integration, has been rigorously verified, and is production proven.

Block Diagram



FEATURES

High Performance 32-bit CPU

- 2.93 CoreMarks/MHz
- Single-cycle instruction execution on most instructions
- Fast and precise internal interrupt response
- Hardware Multiply Unit
- Optional hardware divide, multiply-accumulate, DSP instructions acceleration, and floating-point units

Low Power Consumption

- Industry-leading code density minimizes instruction memory area & power
- From 38,000 sq. µm (or 55K gates) in 28nm technology excluding SRAMs for caches and MMUs.

Fast & Flexible Memory Access

- Harvard-style Caches and MMU separate for Instructions and Data
- Tightly coupled Quick Memory (QMEM) for fast and deterministic access to code and/or data
- Memory Management Unit for virtual memory support

Efficient Power Management

- Dynamic clock gating and power shut-off of unused units
- Software- and hardware-controlled clock frequency
- Wake-up on tick timer or external interrupt

Advanced Debug Capability

- Non-intrusive debug/trace for both CPU and system
- Complex chained watchpoint and breakpoint conditions
- Standard JTAG and proprietary Two-Wire Debug interfaces

Integrated Peripherals

- Base configuration includes a 32 bits-wide tick timer and a programmable interrupt controller
- Optionally pre-integrated with AMBA bus infrastructure, DMAs, GPIOs, UARTS, Timers, SPI, I2C, memory controllers and other IP cores from CAST.

Easy Software Development

- Beyond Studio IDE integrating GNU-based cross-compiling toolchain
- Ported libraries, tools and Oss

www.cast-inc.com • info@cast-inc.com • tel +1 201.391.8300

Engineered by BEYOND SEMICONDUCTOR

The BA2 Instruction Set

The BA2 instruction set provides extreme code density without compromising performance, ease of use, or scalability. It features:

- A linear, 32-bit address space
- Variable length instructions: 16, 24, 32, or 48 bits
- Simple memory addressing modes
- 16 to 32 general purpose registers
- Efficient flow-control, arithmetic, and load/store instructions
- Floating point and DSP extensions

Software Development

The core is delivered with BeyondStudio™, a complete Integrated Development Environment (IDE) for Windows and Linux under Eclipse. BeyondStudio includes a highly featured source code editor, supports graphical source-level debugging and GUI based configuration, and can be extended with a collection of available or custom plug-ins.

The IDE integrates an Instruction level simulator and a GNU cross-compiling tool chain. The GNU Compiler Collection (GCC), includes front ends for C, C++, Objective-C, Fortran, Java, and Ada; libraries for these languages (e.g. libstdc++, libgcj, etc) are provided. The tool chain also includes the GNU Binutils collection of binary tools, and the GNU Project Debugger (GDB).

Extensive support of libraries enables easy application development for Linux and Android. Finally, hardware targets can be interfaced with the cost effective Beyond Debug Key, which in addition to standard JTAG (IEEE 1149.1 and IEEE 1149.7) also supports proprietary One Wire Debug and Two Wire Debug protocols.

Support and Services

The core as delivered is warranted against defects for 90 days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

IP Integration Services are also available to help minimize time to market for BA22-based systems. The processor core can be delivered pre-integrated with typical peripherals such us UARTs, timers and serial communication cores, or with memory controllers and interconnect IP cores. Contact CAST Sales for details.

Implementation Results

The BA22-AP can be mapped to any ASIC technology or FPGA device (provided sufficient silicon resources are available). The following are sample ASIC pre-layout results re-ported from synthesis with a silicon vendor design kit under typical conditions, with all core I/Os assumed to be routed on-chip. Implementation numbers are for the core implemented with 4-way associative cache memories, 4-way associative MMUs and without an FPU.

ASIC Technology	Freq. (MHz)	Area (μm²)	Logic Eq. Gates
TSMC 90nm (wl30, typ)	50	172,701	34,965
	150	179,021	36,245
	200	187,194	37,900

The provided figures do not represent the higher speed or smaller area for the core and area figures do not include the cache and MMU RAM size. Area, power and speed depend on configuration, optimizations, process, and libraries. Furthermore power consumption depends on power management, software and memories configuration. Please contact CAST to get characterization data for your target configuration and technology.

Deliverables

The core is available for ASICs in synthesizable Verilog source code or for FPGAs in optimized netlists. It includes everything required for successful implementation: extensive documentation, a testbench, sample synthesis and simulation scripts, and the BeyondStudio™ Eclipse-based software development IDE for Windows and Linux.

Reference designs on FPGA boards are also available; contact CAST Sales for information.

Related Products

The BA2x™ Processor Family includes a set of royalty-free, pre-configured products intended for different applications:

- **BA20 Pipeline Zero 32-bit Embedded Processor**, an ultra-low power processor using zero pipeline stages for instruction execution to provide maximum energy and performance efficiency.
- **BA21 32-bit Low-Power Deeply Embedded Processor**, a dual-pipeline low-power processor that delivers better performance than most processors its size.
- **BA22-DE 32-bit Deeply Embedded Processor**, a flexible and efficient processor with 4- or 5 pipeline stages that delivers the processing power required for demanding deeply embedded applications.
- **BA22-CE 32-bit Cache-Enabled Embedded Processor**, a 4- or 5-stage pipelined processor, with instruction and data caches.
- **BA25 Application Processor**, a 7/12-stage pipelined, out of order, cache- and MMU-enabled processor.