B16550D

16550D UART

The B16550D is a standard Universal Asynchronous Receiver-Transmitter (UART) providing software compatibility with the popular National Semiconductors 16550D device.

The core encapsulates data provided by the host system to RS232 frames and transmits them over the serial link. On the receive-side, the core assembles received serial data to frames, which are then parsed and the enclosed data are passed to the host system. The B16550D has a complete modem control capability, and a programmable baud rate generator.

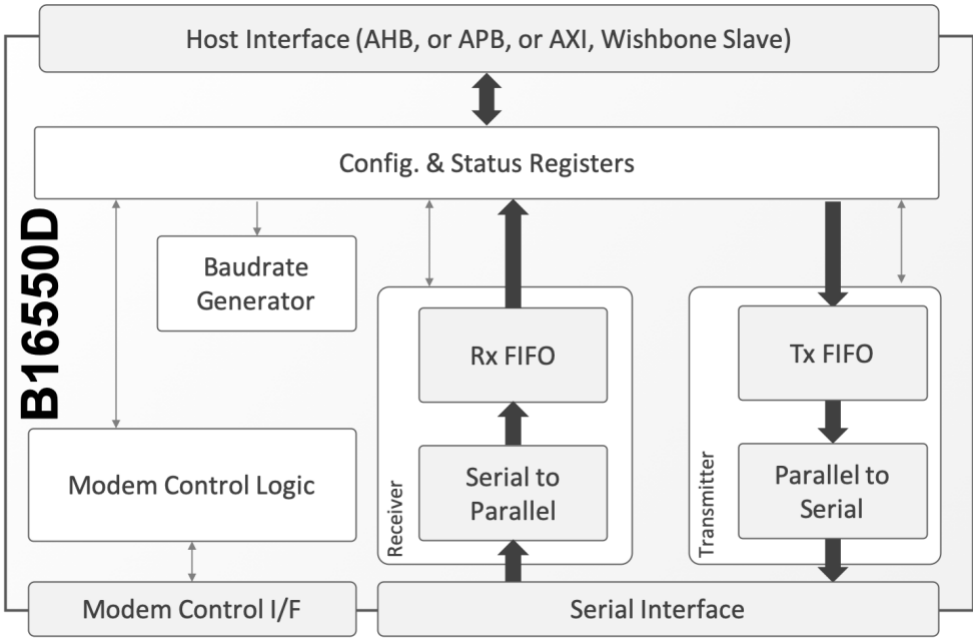
The B16550D can be run in either 16450-compatible character mode or in 16550- compatible FIFO mode, where an internal FIFO relieves the CPU of excessive software overhead. It communicates with the host via an AHB slave interface. A version with an APB, AXI-Lite, or Wishbone host interface can be made available on request.

The UART core is rigorously verified, silicon-proven and available in RTL source or as a targeted FPGA netlist.

Applications

The B16550D core can be used in a variety of serial communication applications including a serial or modem computer interface, or a serial interface with modems and other devices.

Block Diagram



FEATURES

- Compatible with 16450 and 16550D software
- In FIFO mode, transmitter and receiver data are buffered to reduce number of interrupts introduced to the CPU
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from the serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud generator divides any input clock by 1 to (2**16 - 1) and generates the 16x clock
- Modem control functions: CTSn, RTSn, DSRn, DTRn, RIn, and DCDn
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8 bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1, 1½, or 2 stop bit generation
  - Baud generation
- False start bit detection
- Complete status register
- Internal diagnostic capabilities: loopback controls for communications link fault isolation
- Line break generation and detection
- Priority interrupt system control
- No synchronization is needed between the UART core and the CPU because of transmit hold and receive hold registers respectively
- Compile time configurable memory access mode (byte or word)
- AMBA™ AHB Slave host-interface; versions with APB, or AXI-lite, or Wishbone interfaces available up on request

Deliverables

- Synthesizable RTL or FPGA netlist
- Testbench & sample test cases
- Simulation & synthesis scripts
- Documentation

Support

The B16550D as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

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