

AHB2APB

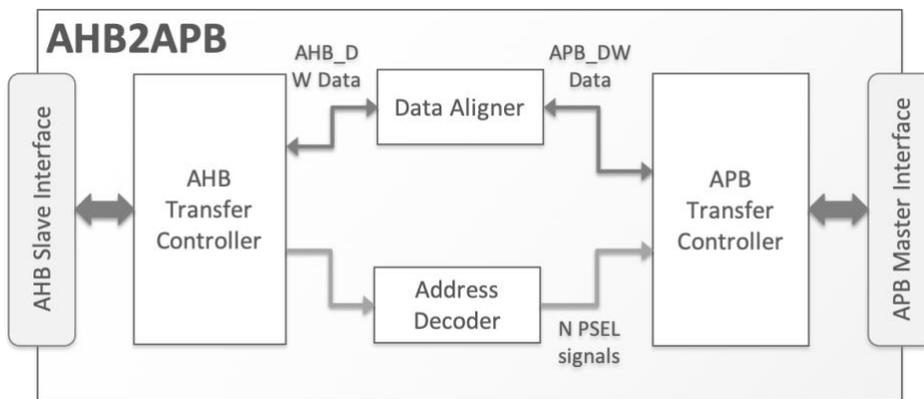
AHB to APB Bus Bridge

The AHB2APB implements an AMBA® AHB to an AMBA® APB bus bridge, allowing the connection of peripherals with an APB interface to an AHB bus.

The highly-configurable core translates read or write AHB bus transactions to APB bus transactions. A full AHB or AHB-Lite master, such as a microprocessor, can connect to its AHB slave interface, and an APB4, APB3, or APB2 peripheral can connect to its APB master port. Furthermore, the endianness and the data bus widths of the AHB and APB interfaces are independently configurable. The user can also select the number of APB slaves and their address mapping at synthesis time. To ease core configuration, the core's deliverables include a software application that enables users to configure the core via an intuitive HTML interface and automatically generate the corresponding Verilog parameter values.

The LINT-clean and scan-ready AHB2APB core is extensively verified and proven in multiple production designs. It can be mapped to any ASIC or FPGA, provided sufficient silicon resources are available, and it is delivered with everything required for successful implementation including a test-bench and comprehensive documentation.

Block Diagram



Support

The AHB2APB as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

FEATURES

AMBA® AHB to APB Bridge

- Allows connecting APB slaves to an AHB master
- Supports full AHB and AHB-Lite masters
- Supports APB4, APB3, and APB2 Slaves

Configuration Parameters

- AHB data bus width and endianness
- APB data bus width (can be different than AHB data bus width)
- APB address bus width
- Number of APB Slaves
- Data width, base address and address space per APB Slave
- Use of PSTRB signal per slave

Easy to Use and Integrate

- Requires no run-time programming or initialization
- HTML configuration tool generates Verilog parameters
- Fully synchronous, scan-ready, LINT-clean design
- Delivered with sample scripts, RTL testbench and sample test cases