# AHB-MLIC

## AHB Multilayer Interconnect

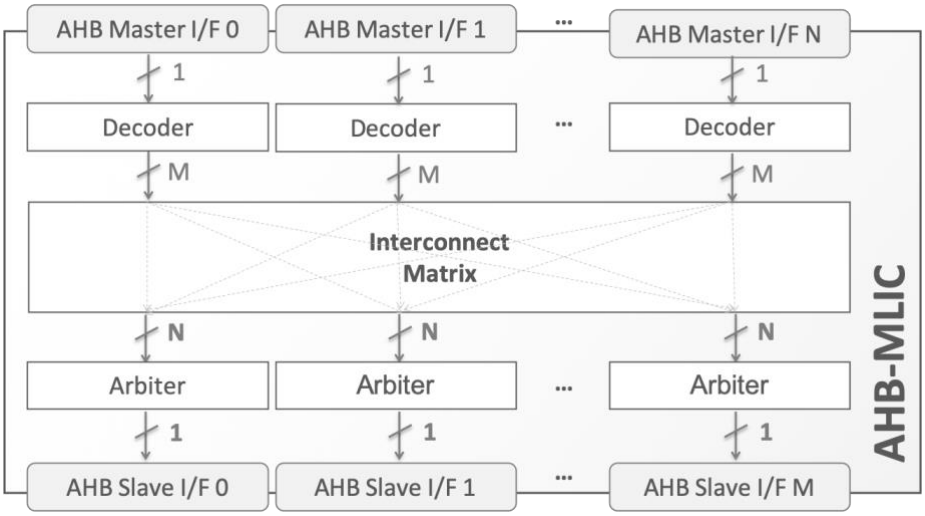
The AHB-MLIC is a multilayer AMBA® AHB bus fabric connecting an arbitrary number of bus masters to an arbitrary number of slaves.

The multilayer fabric offers higher interconnect throughput than a typical AHB bus, as arbitration is performed at the slave port and therefore masters do not compete for bus control. In practice, each master accesses the peripherals connected to the slave ports via a dedicated bus, and only competes with others when they attempt to access the same peripheral at the same time.

The highly-configurable AHB-MLIC allows users not only to define the number of master ports and the number of slave ports, but also to define the slaves' addresses per master port and the arbitration scheme per slave port. Also, it is possible to enable or disable slave access per master. To ease the core configuration, the deliverables include a software application that enables users to configure the fabric via an intuitive HTML interface and automatically generate the corresponding Verilog parameter values.

The LINT-clean and scan-ready AHB-MLIC core is extensively verified and proven in multiple production designs. It can be mapped to any ASIC or FPGA, provided sufficient silicon resources are available, and it is delivered with everything required for successful implementation including a test-bench and comprehensive documentation.

## Block Diagram




## FEATURES

### Configurable AMBA® 3 AHB Interconnect Fabric

- Arbitrary number of AHB-Lite master ports
  - Full AHB masters can also be connected
- Arbitrary number of AHB slave ports
- User-defined slave to master mapping
  - Slaves access can be disabled to one or more masters.
- User-defined slave address per master
  - A slave address can be different between masters.
- Round-robin or priority-based arbitration selectable per slave
- AHB data bus-width (8 to 1024 bits)

### Higher Throughput

- Less arbitration overhead between masters, as arbitration is done at each slave port

### Easy to Use and Integrate

- Requires no run-time programming or initialization
- HTML configuration tool generates Verilog parameters
- Fully synchronous, scan-ready, LINT-clean design
- Delivered with sample scripts, RTL testbench and sample test-cases

## Support

The AHB-MLIC as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.