AC97-CTRL

AC'97 Audio Controller

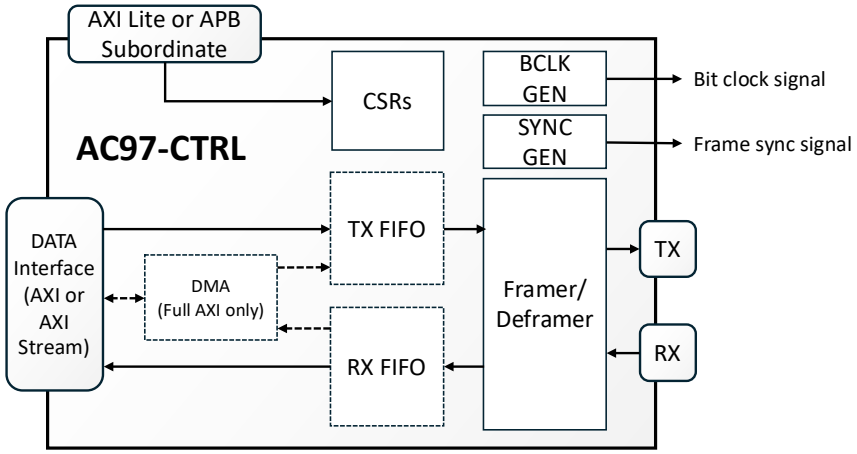
altera™ The AC97-CTRL Audio Controller is a configurable IP block designed to simplify the integration of the AC'97 audio interface into FPGA designs. Fully compliant with the Intel Audio Codec '97 (AC'97) Revision 2.3 specification, this controller facilitates reliable transmission and reception of stereo or multi-channel audio streams using the well-established AC-Link interface. With support for a single codec operating at a standard 48 kHz sample rate, the core is ideal for embedded applications that demand proven audio infrastructure with a compact silicon footprint and efficient data handling.

Control interface options include AXI-Lite, APB, and a generic microcontroller interface, while data transport is enabled through either AXI-Stream interfaces or a controller memory-mapped AXI interface driven by an integrated DMA. This enables both simple streaming applications and use cases requiring block transfers from system memory, such as audio playback from large buffers or real-time audio capture.

The AC97-CTRL core includes a complete set of power, reset, and synchronization management features. Designers can choose the bit clock source (controller or external codec), configure master clock division, and leverage cold/warm reset sequences with programmable timing. A tri-state management scheme ensures proper multi-device behavior on shared AC-Link signals, and interrupt signals provide real-time feedback for underrun and overrun conditions, reducing CPU load and improving reliability in time-sensitive applications.

The AC97-CTRL Controller Core is packaged with everything required for immediate deployment and verification, including lint-clean synthesizable Verilog, testbenches and simulation scripts for 100% coverage, synthesis scripts, Bare-metal driver and example firmware. Its modular architecture and rich configurability make it a strong fit for consumer audio systems, automotive infotainment units, industrial embedded platforms, and any application seeking a mature, standards-based audio interface with minimal integration risk.

Block Diagram



Applications

- **Consumer Audio Systems** such as Embedded PCs, media players, game consoles and laptops.
- **Automotive Infotainment** for Rear-seat entertainment modules, or any system requiring analog audio interfacing
- **Embedded and Industrial Systems** like Point-of-sale terminals, medical devices, or Kiosks and industrial panels

FEATURES

Industry Standard Compliance

- AC'97 Rev 2.3 Compliant
- Full support for single-codec operation at 48kHz sample rate

Flexible Interface Options

- **Control:** AXI-Lite, APB, or generic microcontroller interface
- **Data:** AXI-stream or AXI
- Hardware configurable TX/RX FIFO depths with AXI-stream data interface
- Software programmable internal DMA with AXI data interface

Power, Reset, and Interrupt Management

- Cold and warm reset sequences
- Power-down detection and recovery
- Overrun/underrun detection with configurable thresholds

Multiple Channel Support

- Supports up to 10 transmit/receive audio channels
- Software configurable number of audio channels and channel-slot routing
- Sample depth up to 20-bit, per AC'97 Rev 2.3

KEY BENEFITS

- **Versatile Integration—**Broad interface protocol support simplifies SoC integration.
- **Ease of Use—**Intuitive control/status register map with software driver and example firmware.
- **Reliability**—Clear state machine with reset and power-down logic ensures robust audio data exchange

DELIVERABLES

- Lint-clean synthesizable Verilog RTL
- Simulation testbench and scripts with 100% code coverage
- Synthesis constraints and scripts
- Bare-Metal software driver and example firmware
- Comprehensive User Guide
- **On request:** Linting, synthesis, and verification reports

Size and Performance (Altera)

The AC97-CTRL can be mapped to any Altera FPGA device (provided sufficient silicon resources are available). Its silicon resources requirements depend on its configuration. With a full AXI interface and DMA, it uses approximately 1.5k ALMs. The core interfaces can be clocked at frequencies exceeding 150 MHz in most Altera FPGA devices.

Please contact CAST to get characterization data for your target configuration and FPGA device.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.