



Technical Bulletin

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Verification of IP Integrity

One of the major issues facing customers who wish to purchase IP from a commercial vendor is determining how well the product conforms to specification. IP cores are often software representations of functionality which originally existed in the form of silicon (with specifications in a data book) or which exists solely as a publication of some standards document. The price of commercial IP may be justified for any of several sound engineering tradeoffs, but there is an underlying assumption that the IP behaves exactly to the functional specification. How can a customer gain confidence that a vendor's product truly matches the required functionality? The risks may be intolerably high if it does not.

There are a number of standards and programs being used and promoted through out the IP industry today. Unfortunately, none of them to date represent a widely used, common standard. CAST supports these standards efforts, but to help customers judge our quality today we have provided this bulletin of the methodologies used at CAST to insure the integrity of the IP we provide.

CAST verification methods vary only slightly from one core to the next. The variance is in the form of hardware verification used. The process steps are the same. Before we look at each step, there are two fundamental points to be made.

- All cores are provided with simulation vectors and a test bench. The vectors are the fundamental proof of the functionality. The test bench is the tool that allows the customer to verify that the required functionality is available in the core.
- All cores are hardware verified. The same vectors that run in the testbench are run against actual silicon that represents the required functionality. The outputs from the core must match those from the silicon or the standard on a cycle-by-cycle basis. Now let us look at the process used in developing a high quality core.

The first key to a high quality core is careful planning and set up. The development engineer must thoroughly understand the required function and must lay out a modular development approach to facilitate both coding the core and developing the test vectors that will be used to verify functionality. Unless testing and verification are considered from the beginning, developing a proper set of vectors will become next to impossible. More likely, a less than robust set of vectors will be developed and verification will be shoddy. During the planning process, a target device (existing, off the shelf silicon) that best represents the functionality being developed is chosen. This is the device that will be used during the hardware verification process.

Actual core development begins next following CAST internal coding standards that have been developed based on hundreds of man-years of experience writing HDL code. As is true in any complex technical development, experience counts. CAST is one of the oldest suppliers of commercial IP in the market having been founded in 1993. We use our experience in both our internal core developments and in choosing our business partners. One of our major partners, Evatronix SA of Poland, has been working with us for over four years and shares our development methodology and tools. They were originally selected as a partner because of their commitment to quality and philosophical compatibility with CAST.

After each module is developed, the test vectors are generated. This has proven to be the most efficient way of developing a high quality test. Once the vectors exist, they are run against the core code and code coverage tools are used to determine whether the entire functionality of the module is being exercised. The importance of using code coverage tools cannot be overstated. Similar to fault simulation in the early days of simulation, these tools provide the only objective measure of the vector's validity. These tools verify that each HDL statement has been exercised at least once by the vectors.

Once the development process is complete, hardware verification begins. The device that was originally chosen as the example of the desired functionality is built into a test board containing the circuitry necessary for it to function. In many cases, particularly those where the device may be obsolete, CAST has a unique advantage. Because of our unique heritage as a simulation and tools provider, we have access to hundreds of hardware models for older devices plus the hardware modeling tools to run them. Using these tools whenever possible gives us a powerful way of verifying devices that might otherwise be impossible to hardware verify. Whatever hardware tool is used, the key verification technique is to compare the results from running the test vectors developed earlier against the physical target and against the core running in a simulator. These results must match. Logic analyzers and other timing analysis tools are also used to verify timing as well as functionality. It should be noted that our cores are developed to be independent of any particular silicon supplier or process. The exact timing in an application will depend on the specific choice of silicon. If timing tolerances are fixed, as in many legacy application conversions, the customer should consult with CAST's engineers concerning application details. Because of our careful attention to detail in the verification process, we may be able to provide guidance on the best approach to a successful implementation. Depending on the complexity of the device under development, an extra step may be added. A physical implementation of the core in an FPGA may be done for further testing. This is generally the case when the core represents a device where there are published standards or tests. This becomes the final step in the process. If the core in the FPGA can be plugged into the test bench and the same results achieved, we know we have achieved our goal of building the most risk free product possible.

The last phase required before shipment is the documentation phase. All aspects of the core's functionality, the test bench, and the vectors must be documented in a clear professional manner. Once this is accomplished and reviewed, the core is considered released for shipment.

CAST's goal is to deliver the most risk free cores possible. Given this rigorous methodology, CAST's customers have a confidence that their use of our commercial IP will be one of their best investment decisions.

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