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Reference Design Paper

A New Reference Design Development Environment for JPEG 2000 Applications

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Abstract
The newest revisions to standards for video processing, like JPEG and MPEG are becoming available and are expected to create new applications and markets. Hardware implementations of these standards will be available first in the form of IP Cores for FPGAs. A reference design based on a Xilinx FPGA development board from Avnet Design Services and IP Cores from CAST have been combined to create a reference design for the newest versions of the JPEG and MPEG standards. The paper will describe the features and functionality of the design as well as the size, performance and cost of the final circuit board implementation. This Reference Design will be demonstrated in the Reference Design Village.

Authors' Biographies
Bill Finch
Bill attended Purdue University where he received a BSEE in 1969. Out of Purdue he joined GenRad, Inc. as a sales engineer and rose through the sales ranks to become US Sales Manager in 1981. Two years later he became Product Line Manager for a new product in functional testing of microprocessors. Mr. Finch held a variety of executive positions at GenRad in product management and marketing until he left in 1995 to join Boreas, Inc., a start-up in the field of Superconductivity. He has been VP of Sales and Service for SemiTest, Inc. , a supplier of metrology tools to semiconductor firms such as Intel and Motorola. He was President and General Manager of the Surface Inspection Systems division of Brown and Sharpe that specialized in defect detection in semiconductors and flat panel displays. He has been vice President of Sales for CAST for the last two years.

Warren Miller
Warren is Vice President of Marketing and Honorary Chief Engineer at Avnet Design Services. He is responsible for managing the centralized applications design center, technical marketing and business planning efforts for Avnet Design Services, the technical arm of Avnet Cilicon, the premier technical distributor of complex semiconductor products. Warren has worked in the electronics industry for over 20 years as a design engineer, applications engineer, and Director of Engineering as well as in marketing, so he can both code in and spell VHDL.

Introduction

The ability to send images of all sizes and types quickly from Point A to Point B has long been viewed as one of major benefits of high-speed networks and the Internet. However, in spite of the huge advances in compute power and network bandwidth, we are still short of realizing the goal. Large, complex images still defy us if we want to get a true reconstruction of the original at the receiving end without tying up our networks for long periods. We still need to manage multiple formats and support multiple tools to encode and decode these formats. The ability to manipulate the image during transmission is totally missing.

With the publishing of the JPEG 2000 standard in 2001, we are now much closer to achieving our goals. JPEG 2000 is a single standard that allows for highly scalable applications aimed at satisfying most users. The advantages of the new standard are:

- Better image quality at the same file size
- 25-35% smaller file sizes at comparable image quality
- Good image quality even at very high compression ratios, over 80:1
- Low complexity option for devices with limited resources such as cellphones
- Scalable image files -- no decompression needed for reformatting. With JPEG 2000, the image that best matches the target device can be extracted from a single compressed file on a server. Options include:
    i. Image sizes from thumbnail to full size
    ii. Grayscale to full 3 channel color (there is no limitation in the number of color channels –e.g. there are satellite images with 4 and more olor channels)
    iii. Low quality image to lossless (identical to original image)
- Progressive rendering and transmission through a layered image file structure. Example: from a single 100 KByte image file of a 512x512 original image, a low resolution 32x32 pixel thumbnail image can be transmitted by sending only 10Kbytes. Sending an additional 15 KBytes increases the resolution to 64x64 pixels, and so on. Other layerings provide for progressive transmission and rendering based on quality, color component and spatial location in the image.

With these tremendous advantages an increasing number of designers will be developing applications using these standards, but the design engineer may not have a lot of time to do the detailed design and compliance testing- they may need a reference design platform and intellectual property that can leverage design time. This paper will describe just such a reference design.

JPEG2000 Application Description

The big differences with past compression techniques are in the use of Discrete Wavelet Transforms to de-correlate the image prior to compression and the ability to have multiple entropy coders (the “real” compression engine) to achieve high throughput. Most of the bottleneck in the past has been in the entropy coders. Approximately 70% of the time spent encoding an image is in this phase. The ability to separate the actual bit stream from the data about the construction of the bit stream is critical to the ability to manipulate the image as desired with out changing the underlying stored image itself.

By controlling parameters such as the type of filtering done in the DWT and the quantization levels, we can achieve everything from lossless transmission at low compression ratios to lossy transmission with very high compression (200:1) while still controlling image quality.

Given the number of factors involved, it is important to consider the following key trade-offs in a design.

Throughput required, Image size(s) to be processed, Image composition (color, mono, etc.), Lossy vs. lossless, Implementation technology- FPGA vs. ASIC, and Memory

Now let's consider some specific types of real world design trade-offs, but first lets provide a few more definitions.

- Quantization – This setting allows you to throw away the least significant bits of the transformed image. It basically controls speed vs. resolution.
- Bit rate control – This is an algorithm that selects which part of a compressed image needs to be transmitted for optimum image reconstruction assuming there are bandwidth limitations which don't allow the transmission of the whole compressed image.
- Error resiliency – Mechanisms are built in to the standard to allow recovery from errors in transmission. This is especially important in noisy transmissions, e.g. wireless.

Now for the trade-offs:

- Speed vs Area (and memory requirements)
  - The standard allows for code-blocks to be entropy-coded / decoded separately. Therefore, parallel entropy coding engines can be employed to increase speed. This comes, of course, at the cost of extra memory and area (gatecount).
- Speed vs "optimal" bit-rate control
  - The time spend in entropy coding (which is a large fraction of the total encoding time) can be reduced if less data are fed for entropy coding. This can be achieved by using higher quantization values. However, the bigger the quantization values are, the smaller the optimization field is left for the bit-rate control algorithm.
- Programmability vs Area
  - Hardwiring the DWT filter type (5/3 or 9/7), the quantization tables, and the entropy coding switches can help to reduce the area requirements.
- Error resilience vs Compression efficiency (bandwidth)
  - Error resilience mechanisms introduce small overheads in the final stream size.

Reference Design Platform

Given the number of issues for a designer to consider and the fact that the standard is still relatively new, the need for a robust but easy to use development environment becomes obvious. It is much easier for a design engineer to learn about JPEG 2000 and experiment with the effects of the various trade-offs using real world images and live hardware. Designs get to market faster and with less effort. CAST, Inc. has teamed with Avnet Design Services to bring to market just such a reference design and development environment based on the CAST JPEG 2000 IP core and the Avalon reference design boards from Avnet.

Figure 1 shows a block diagram of the JPEG2000 IP Core from CAST. The core implements all the key elements of the JPEG2000 standard. The primary interfaces are the pixel interface, the buffer memory interface and the host interface. Inside the core are the DWT engine, the entropy coding engines and the required support logic for control, arbitration and quantization. A hardware development board for

Avnet Design Services, shown in figure 2, can be used to demonstrate the functionality of the JPEG2000 IP core.

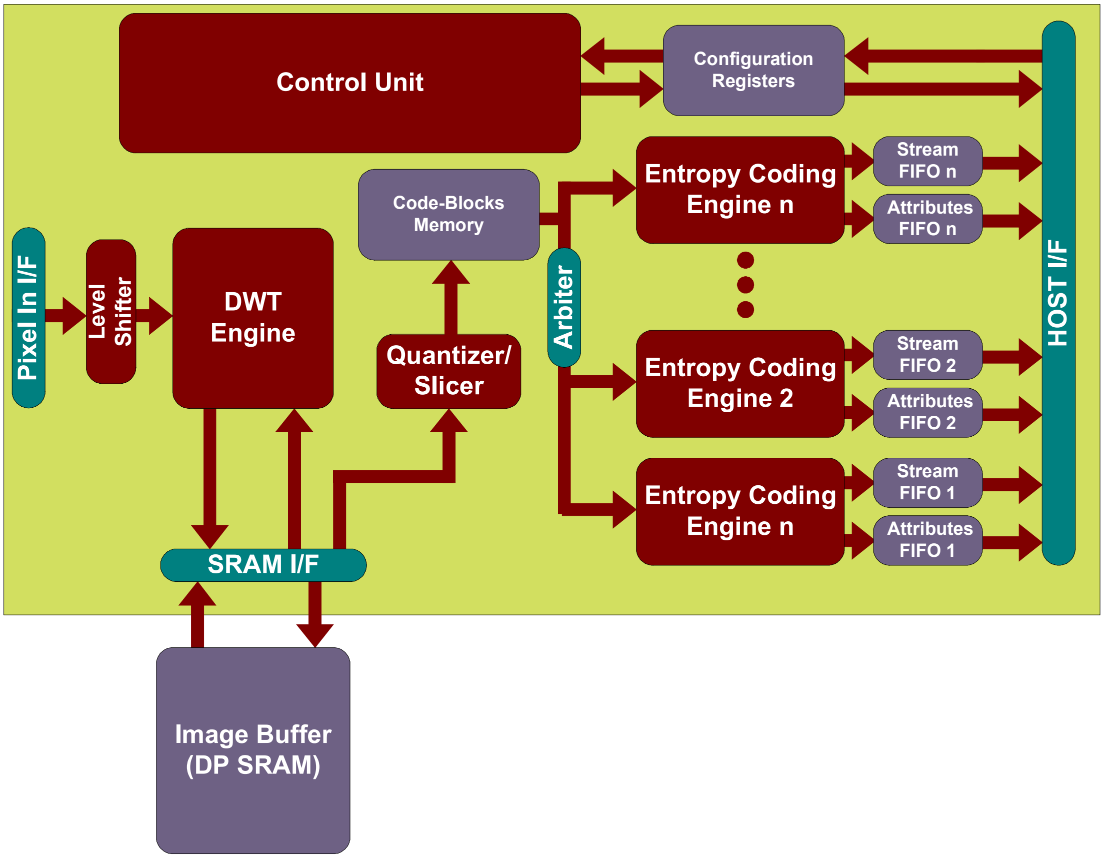

Figure 1: JPEG2000 IP Core from CAST Block Diagram

The Virtex II based development board provides an ideal platform for developing complex, high performance designs. It offers a huge FPGA with more than sufficient amounts of internal (high-speed) memory. It offers easily expanded external memory that can be used for the non-time-critical buffering.

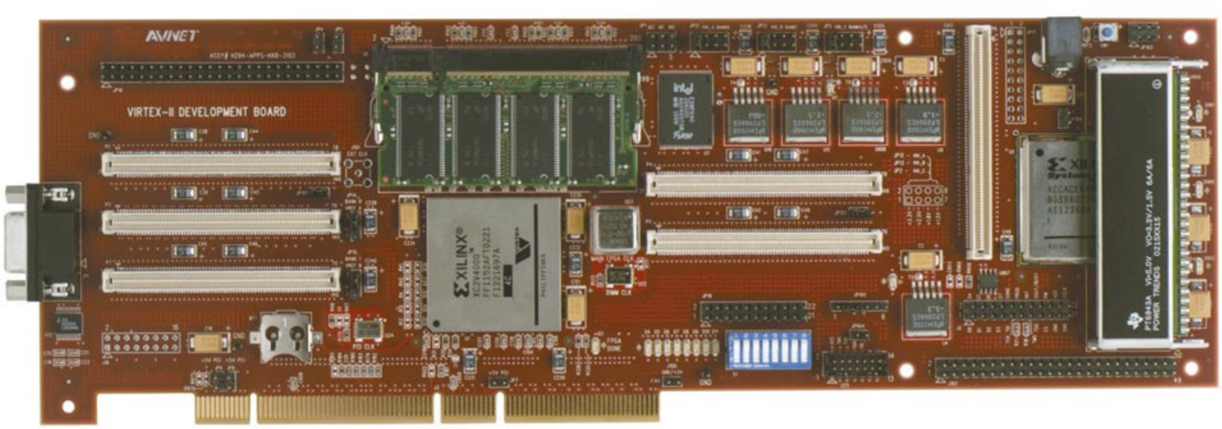

Figure 3: Demonstration Application- JPEG2000

It offers a high-speed link to the host CPU through a PCI bus interface. Lastly, for live data input it offers a generic video interface via a daughter board. Other Avalon options exist for different types of applications for the core, but since most of the time engineers want to push the envelop of the technology, we chose the Virtex II. All of this backed by excellent support makes the choice a simple one.

Ordering Information

The JPEG2000 IP Core and Virtex-II development board can be ordered from Avnet Design Services. For information on price and delivery visit the ADS web page at www.avnetavenue.com.