

CAST

PIP-AMBA-E

SoC Kernel for ARM9 AMBA Bus Systems

The PIP-AMBA-E provides the essential IP cores and infrastructure software needed for systems using a microprocessor from the ARM 9 family with the AMBA bus, a de facto open standard. Ready for software development out of the box but also easy to customize and extend, it serves as a basic platform for the rapid development of a variety of system-on-chip (SOC) applications.

The platform is well suited to a variety of AMBA-based SoC designs. It includes the multi-master and arbitration features of the high-performance AHB bus, and a bridge to the slower APB peripherals bus. The architecture makes it straightforward to add additional IP cores or custom logic to either bus.

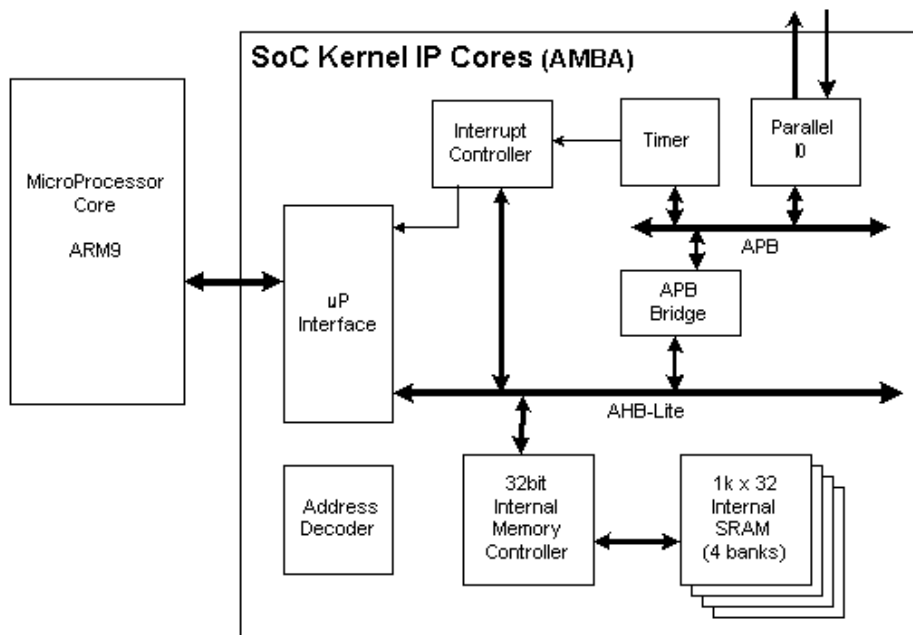
The platform includes synthesizable HDL cores for the AHB and APB buses, plus various timers, controllers, interface functions, communications functions, and an internal SRAM block. (FPGA netlist versions are also available.)

Generous standard deliverables include Software device drivers, boot code, service routines, and support for an embedded real-time operating system (RTOS). The included SOC test and validation suite features an AMBA Bus Functional Model.

Applications

The platform is suitable for small microcontrollers and mixed-signal controllers for a variety of applications, including factory automation, automotive systems, hand-held devices, motor controls, and intelligent toys.

Block Diagram



Features

- Integrated IP cores and software subsystem provides basic infrastructure for many SoC applications
- Platform saves significant time over acquiring and integrating separate elements
- Works with low-power, 32-bit ARM 9 processors
- Built on AMBA standard bus for broad applicability
- Enables both the high-performance AHB and the APB peripherals buses
- Easily add custom logic or additional IP cores to tailor or expand the system
- Immediately begin software development and test
- Supports ARM® RealView®, GNU and other development tools
- Complete infrastructure includes essential hardware and software
- Included IP cores:
 - Microprocessor interface
 - APB Bridge
 - Timers
 - Scalable Interrupt Controller
 - Parallel I/O
 - Internal SRAM with Controller
- Software
 - boot code
 - Interrupt Service (ISR) code
 - Main code with Scheduler
 - Device driver code
 - Hardware Level API
- Plug-in architecture for user-defined custom IP blocks
- Support for real-time operating systems (RTOS)
- Comprehensive SOC test and validation suite, including:
 - AMBA Bus Functional Model with support for interrupts and subroutines
 - Sophisticated HDL Testbench with external models and interfaces
 - System Level Simulation scripts, C-test/Macro test code and comparison utilities
- Complete user documentation

Functional Description

The PIP-AMBA-E is a completely integrated and tested platform, including the bus system, memory system, and peripherals. It includes two AMBA-standard buses: AHB for high-speed transactions such as local memory access or DMA operations, and APB for slower transactions with peripherals such as UARTS and the GPIO. Users can readily add their own custom logic or other IP cores. The included cores and software are as follows.

IP Cores

Microprocessor Interface

Communicates between the AHB bus within the platform and the Microprocessor bus.

Address Decoder – Memory Map

The Memory Map is easily configurable using HDL Header Files. The Address Decoder supports AMBA decoding on the AHB and APB buses.

Interrupt Controller

Manages processor attention requests for the RTOS. Fully scalable to support from one to 32 interrupt sources, and provides a programmable register used when generating an interrupt under software control.

APB Bridge

Serves as an interface between the AHB and APB buses, and is a slave to the AHB. Transactions targeted at slow peripherals on the APB are initiated on the AHB, translated to APB bus cycles, and returned to the AHB via handshaking signals.

Timers

The 16-bit counter/timers are necessary for any RTOS needing a timebase and scheduling. They are fully programmable and include selectable prescale values of 1, 16, and 256. Two modes of operation provide a free running value and also periodic interrupts.

Parallel IO

Configurable, Parallel I/O module with a scalable set of up to 32 I/O lines. Each line can be configured independently of the others, with any combination of inputs or outputs.

SRAM Controller and SRAM

The Internal SRAM Controller provides a method of communicating with an integrated Synchronous Static Random Access Memory (SSRAM). The memory interface allows word, half-word, or byte wide addressing.

Software

Boot Code

Main program setup and entry; low level interrupt handling and setup; memory allocation; stack setup, reset, exception entry vector functions are included in the Boot Code.

Interrupt Service Routines (ISR)

Save and Return pointers to and from Interrupt stack and Interrupt Service Routine entry and exit C-Code functions.

Main Routine with optional Task Scheduler

“Main Function” C-Code includes entry from Boot Code initialization along with an optional timer based priority encoder and task multiplexor.

Peripheral Driver Code

Peripheral Driver Code includes drivers for the Interrupt Controller, Timer, Parallel IO and Memory Controller.

Hardware Level API

The Hardware Level API is easy to understand MACROs that make calls to hardware memory or registers, enabling ease of coding and verification in Simulation and Prototype Emulation environments.

Support

The platform as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The platform has been verified through extensive simulation and rigorous code coverage measurements, and is in use for several customer applications. SoC development kits are available.

Deliverables

The platform includes everything required for implementation:

- HDL RTL source code for the included cores (post-synthesis EDIF netlists for FPGAs are also available)
- Essential software, including boot code and device drivers
- An AMBA Bus Functional Model, Sophisticated HDL and C-Code Testbench, including external models and interfaces
- System Level Simulation scripts, C-test/Macro test code and comparison utilities.
- Comprehensive user documentation, including detailed specifications and a system integration guide.