SOC-Wdog-APB

Watchdog Timer Core

Features

- 16 bit down counter
- 2 selectable prescalers
- Watchdog reset
- Warning interrupt before reset
- Configurable time lapse after reset
- AMBA APB interface

The SOC-Wdog-APB Watchdog Timer is a fail/safe function used to reset a system in case the microprocessor gets lost due to address or data errors.

The Watchdog Timer module is a 16 bit down counter with a selectable prescaler, watchdog reset, warning interrupt, and reset controller. Prescale values of 1, 16 and 256 can be selected. The prescaler extends the timer's range at the expense of precision. Watchdog reset can be used to reset a system after a configurable time lapse without activity. A warning interrupt can be issued a predetermined amount of time before a watchdog reset to indicate a reset is imminent. The reset controller within this module can be used to provide a glitch free version of an external reset to the internal system, and issue an early reset to components before a processor reset.

The SOC-Wdog-APB contains several configuration registers that can be written and read by the processor. Two 4-bit prescalers precede a 16-bit counter. The counter can be clocked at either the input clock rate, or a choice of 2 prescaled rates. The counter can be loaded with a value from a preload register. The watchdog will generate an interrupt when it decrements to the warning time, then a reset when it decrements to zero.

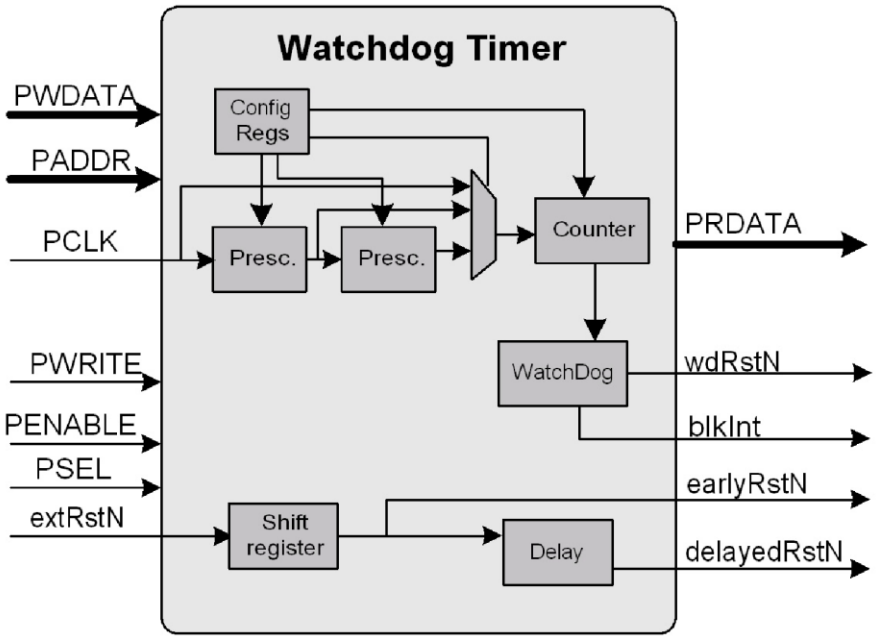
Deliverables

The SOC-Wdog-APB Watchdog Timer package includes fully tested and verified Verilog source and Verilog testbench. The SOC-Wdog-APB can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGAs

Support

The SOC-Wdog-APB core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Block Diagram



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