The IPC-UART-APB is a 16450/16550 compatible Universal Asynchronous Receiver/Transmitter (UART). The IPC-UART-APB contains a baud rate generator that can be configured to generate a wide range of baud rates depending on the system clock frequency and the programmable divisor. The baud rate generator also generates the clkBaud output signal which can be used to provide a timing reference to external receivers. The IPC-UART-APB has 16 byte internal FIFOs for both receive and transmit modes.

There are 12 internal registers for monitoring and control of the UART functions. Status information can be read at any time during operation. The IPC-UART-APB has a prioritized interrupt system which can generate five types of interrupts: receiver line status, received data available, character timeout, transmitter holding register empty, and modem status. The IPC-UART-APB can transfer parallel data via two direct memory access modes (DMA) and has a loopback mode for on-chip diagnostics.

The IPC-UART-APB contains an AMBA APB bus interface.

Deliverables

The IPC-UART-APB package includes fully tested and verified Verilog source and Verilog testbench. The IPC-UART-APB can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGAs.

Support

The IPC-UART-APB core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Block Diagram