



# SOC-Timer APB

## Counter-Timer Core

### Features

- 16 bit counter/timer
- Two 4-bit pre-scalers
- Configurable
- Free running or periodic mode
- Interrupt output
- AMBA APB bus interface
- Testbench

The SOC-Timer APB is a programmable 16-bit counter/timer. The **SOC-Timer APB** was designed for a time-base generator for AMBA based SOCs and for applications requiring an interval timer. The timer function is necessary for any embedded microprocessor based SOC that is running a Real Time Operating System (RTOS).

The SOC-Timer APB Timer module is a sixteen bit down counter with a selectable prescaler. Prescale values of 1, 16 and 256 can be selected. The prescaler extends the timer's range at the expense of precision. The Timer provides two modes of operation that provide a free running value and also periodic interrupts.

The Timer contains several configuration registers that can be written and read by the processor. Two 4-bit prescalers precede a 16-bit counter. The counter can be clocked at either the input clock rate, or a choice of 2 prescaled rates. The counter can be loaded with a value from a preload register. The counter can optionally generate an interrupt.

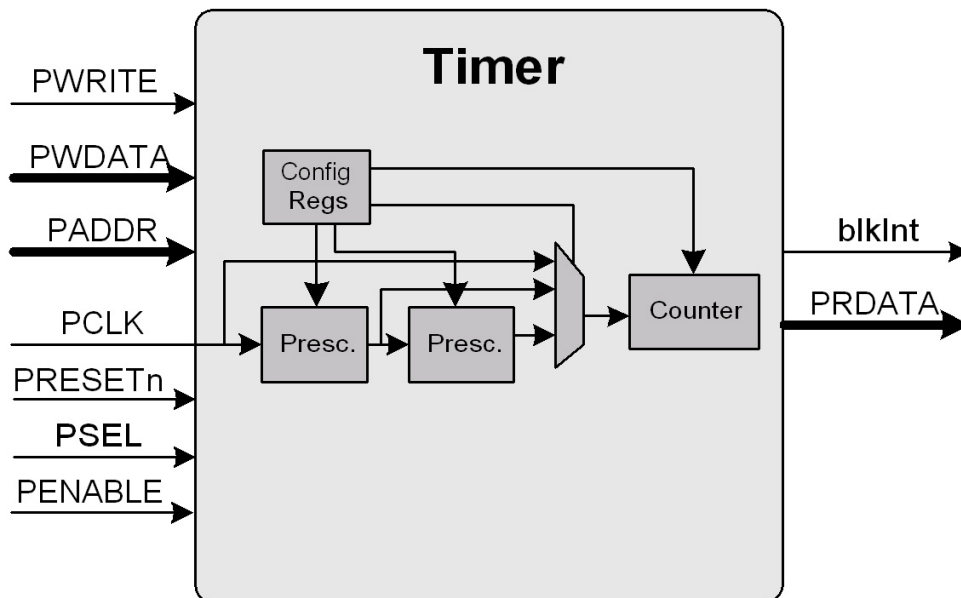
### Deliverables

The SOC-Timer APB package includes fully tested and verified Verilog source and comprehensive Verilog testbench. The **SOC-Timer APB** can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGAs.

### Support

The SOC-Timer APB core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

### Block Diagram



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