



SOC- SRAMCtrl-AHB

Internal Synchronous SRAM Controller Core

Features

- Byte, 16 bit half-word, or 32 bit word access
- AMBA AHB compatible
- Fully scalable
- Optional Byte steering logic

The SOC-SRAMCtrl-AHB, Internal SSRAM Controller, provides a method of communicating with an integrated Synchronous Static Random Access Memory (SSRAM). The SSRAM array comes in byte, half-word (double byte), and word (four bytes) widths and various depths. The default configuration is two kilowords where each word is 32 bits wide (2K x 32). The memory interface allows word, half-word, or byte wide addressing.

The SOC-SRAMCtrl-AHB is compatible with AMBA AHB bus systems.

Deliverables

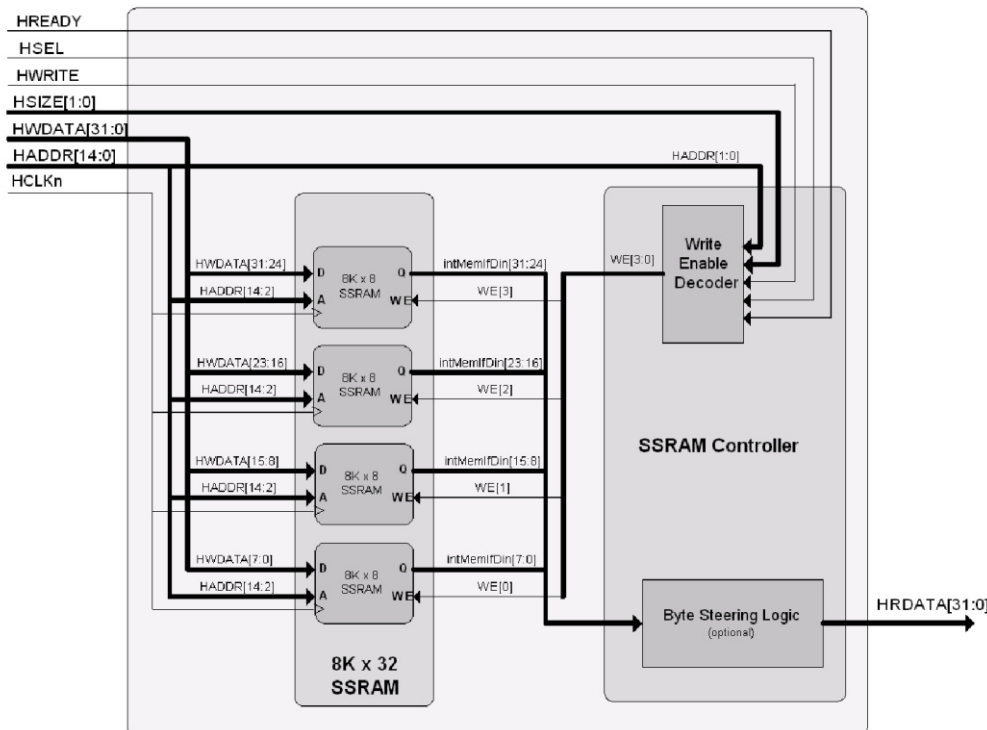
The SOC-SRAMCtrl-AHB SSRAM Controller package includes fully tested and verified Verilog source.

The SOC-SRAMCtrl-AHB can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGAs.

Support

The SOC-SRAMCtrl-AHB core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Block Diagram



April 2008