

# CAST

SoC<sup>TM</sup>Solutions

## SOC-RTC-APB Real Time Clock Core

### Features

- Clock/Calendar (BCD Format)
  - Seconds
  - Minutes
  - Hours
  - Days
  - Months
  - Years
- Alarm Mode for each "Time Unit"
- Repeat Alarm Mode for each "Time Unit"
- AMBA APB Interface
- Interrupt control for Alarms

The SOC-RTC-APB is a clock-calendar IP core that keeps track of the "Time of Day". The core is organized as a series of BCD counters that counts Seconds, Minutes, Hours, Days, Months and Years (Time Units).

The RTC seconds counter time base is generated from a programmable divisor of the system clock. The divisor should be set to generate a 1Hz clock enable signal to the seconds counter. This divisor can also be used to adjust the clock accuracy by periodically adding or subtracting values from the divisor. Calibration accuracy is controlled by software.

Each of the Time Units can be loaded by writing BCD information to the proper Time Unit register. The RTC will immediately load the new time and will continue to count.

The Core can also be loaded with an Alarm Compare value for each Time Unit that will generate an interrupt when that Time Unit reaches the compare value. A Repeat Alarm function is also available. When enabled, this function will cause an interrupt at the terminal count of each Time Unit counter. For example, if the Repeat Alarm bit (bit 7 or Seconds Alarm Register) for the Seconds counter is set, the RTC engine will generate an interrupt every second when the counter rolls over from 59 to 00.

Testmode bits for each Time Unit counter enable the counter to be clocked by the secondsClk in order to speed testability. This can also be used to incrementally update the RTC. The testRstN bit enables the RTC counters to be reset under software control. Otherwise the RTC counters are free running and do not reset upon system reset.

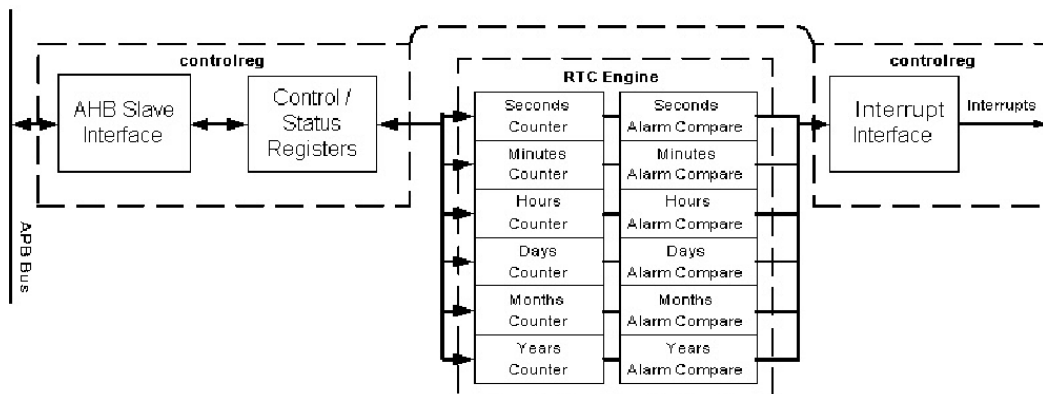
The SOC-RTC-APB operates as a slave device on the AMBA APB bus. Each register is accessed by simple APB bus transactions.

The SOC-RTC-APB package includes Verilog source and simulation test-benches. The SOC-RTC-APB can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGA.

### Support

The SOC-RTC-APB core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

### Block Diagram



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