The SOC-PWM-APB is an AMBA APB core that can be used for motor control, signal modulation, tone generation and any control requiring a variable duty cycle and variable frequency signal.

The SOC-PWM-APB generates a variable duty cycle output signal under program control. The period of the output signal is determined by using a direct counter method or prescaled counter method. The prescale values are PCLK / 256 and PCLK / 4096.

The SOC-PWM-APB duty cycle is determined by accumulating the counter values compared with the value programmed in the dutyCycle register. For example, when the 8-bit counter value reaches the value programmed into the dutyCycle register, the pulseOut signal goes low. When the counter has reached its maximum value and rolls back over to zero, the pulseOut signal goes high.

**Deliverables**

The SOC-PWM-APB package includes fully tested and verified Verilog source. The SOC-PWM-APB can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGAs.

**Support**

The SOC-PWM-APB core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.