



# SOC-ParPort-APB

## Parallel-Printer Port Core

### Features

- 8-bit bi-directional port
- PC printer controls
- GPIO compatible
- 2 interrupt modes
- AMBA APB interface

The SOC-ParPort-APB is an 8-bit bi-directional parallel port compatible with PC printers. The status and command registers provide information about state of the printer inputs and outputs, while the control register allows the programmer to control the printer outputs.

The SOC-ParPort-APB has two bi-directional modes to control I/O for the parallel port. One mode allows the I/O select register to control the parallel port direction while the other mode allows for a direction bit in the control register to control the direction.

The SOC-ParPort-APB provides various printer signals which can be monitored and controlled through the status, command, and control registers. Printer input signals (errorN, slct, pe, ackN, busyN) can be monitored through the status register, printer outputs (strobeN, autoFdXtN, init, slctInN) can be controlled and monitored through the control and command registers respectively.

The SOC-ParPort-APB also provides two interrupt modes, "latch" and "acknowledge". In "latch" mode, the interrupt is asserted on the falling edge of ackN input and will remain set until the status register is read. In "acknowledge" mode, the interrupt tracks the ackN input. When ackN is low, the interrupt will be asserted, and when ackN is high, the interrupt will be clear.

The SOC-ParPort-APB can also be used for general purpose I/O.

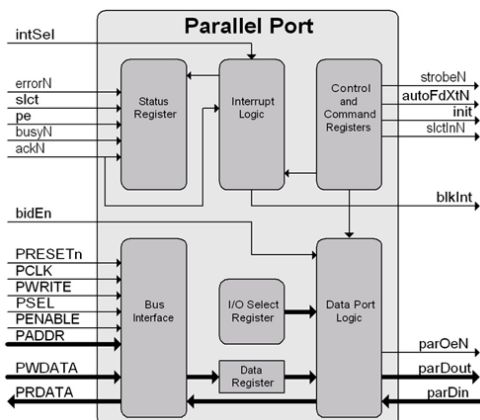
### Deliverables

The SOC-ParPort-APB package includes fully tested and verified Verilog source. The SOC-ParPort-APB can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGAs.

### Support

The SOC-ParPort-APB core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

### Block Diagram



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