



SOC-GPIO-APB

General Purpose I/O Core

Features

- Configurable I/O lines
- Scalable
- Interrupt output
- Selectable level sensitive or edge triggered interrupt system
- Supports asynchronous inputs
- AMBA APB bus interface

The SOC-GPIO-APB is a configurable AMBA APB General Purpose I/O core. The SOC-GPIO-APB is scalable up to 32 I/O lines. All lines can be configured independently of each other, with any combination of inputs and outputs. This module can be used in a wide variety of applications where simple I/O control is needed.

The SOC-GPIO-APB provides synchronization logic for its inputs in order to safely connect with asynchronous inputs or inputs from other clock domains. Optionally the GPIO module can be configured to generate an interrupt on a high level, low level, positive edge, negative edge, or either edge of any general purpose input line. Each input line has a dedicated interrupt enable set and interrupt enable clear register. Each line configured as an output also has dedicated set and clear registers for simple output control. If interrupt capabilities are not required, the GPIO can be conditionally compiled without interrupt capabilities to save gates.

All signals needed to implement a bidirectional bus are provided by the SOC-GPIO-APB.

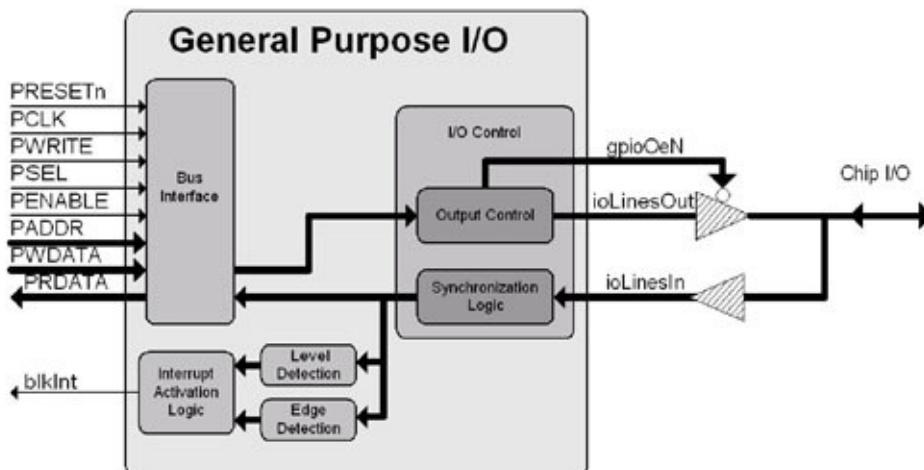
Deliverables

The SOC-GPIO-APB General Purpose I/O package includes fully tested and verified Verilog source and Verilog testbench and simulation scripts. The SOC-GPIO-APB can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGAs.

Support

The SOC-GPIO-APB core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Block Diagram



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