SOC-EBI-AHB
External Bus Interface Core

The SOC-EBI-AHB External Bus Interface is a configurable module designed to interface an AMBA AHB bus to a generic External Bus. The external bus interface (EBI) allows the processor to transmit and receive data to and from external devices, one or more of which may be memory. External memory can be SRAM, Flash, etc. The user can configure (or program) the SOC-EBI-AHB to the proper number of read and write wait states and the memory size to allow proper communication. The SOC-EBI-AHB allows word, half-word, and byte width addressing to 32-bit, 16-bit, and 8-bit external devices.

The SOC-EBI-AHB interfaces the AHB bus to up to 4 external devices. The HDL source was designed to allow the user to easily scale the EBI to accommodate more than 4 devices. Each device has a configuration register. The 2 LSBs of the address bus are modified depending on the type of access specified by the processor and the capabilities of the device (as programmed into the configuration register). The EBI logic performs this and other tasks such as:

- breaks down device enables into upper, upper middle, lower middle, & lower bank chip enables
- steers data bytes or halfwords onto appropriate data bits
- sequences multi-byte or multi-halfword read and write operations
- puts the processor in a wait state until the access completes

Deliverables

The SOC-EBI-AHB package includes fully tested and verified Verilog source and Verilog testbench. The SOC-EBI-AHB can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGAs.

Support

The SOC-EBI-AHB core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.