



SOC-ApbBridge-AHB

AMBA AHB to APB Bridge Core

Features

- AMBA AHB Slave
- AMBA APB Master
- Adaptation of APB bus signals to AHB bus signals
- APB address decoding
- APB read data bus multiplexing
- Isolates AHB from APB

The SOC-ApbBridge-AHB is used to translate AMBA AHB signals to AMBA APB signals. The SOC-ApbBridge-AHB is also used to isolate the high performance AHB (system bus) from the slower APB (Peripheral Bus).

The SOC-ApbBridge-AHB is an AHB slave component which accepts transactions targeting an APB peripheral, decodes the address, and provides an APB, peripheral bus, transaction to the targeted peripheral or memory.

The SOC-ApbBridge-AHB can decode up to sixteen APB peripherals. On write transactions, the SOC-ApbBridge-AHB provides the write control (PWRITE), select (PSEL), address (PADDR) and data (PWDATA) to the targeted peripheral or memory. On read transactions, the SOC-ApbBridge-AHB multiplexes the targeted peripheral's data (PRDATA_device) to the AHB HRDATA with the proper timing.

The SOC-ApbBridge-AHB also returns the HREADYOUT signal back to the AHB master to indicate that the SOC-ApbBridge-AHB has completed the APB transaction and the data is ready.

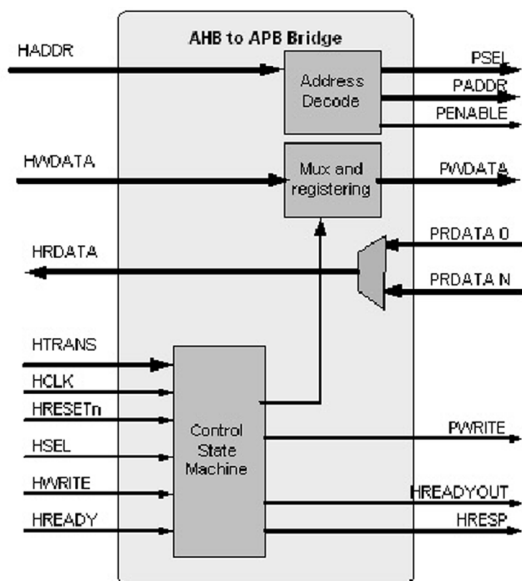
Deliverables

The SOC-ApbBridge-AHB package includes fully tested and verified Verilog source. The SOC-ApbBridge-AHB can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGAs.

Support

The SOC-ApbBridge-AHB core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Block Diagram



April 2008