



SOC-Arbiter-AHB

AMBA AHB Arbiter Core

Features

- Round robin priority
- Scalable (Up to 16 masters)
- AMBA AHB interface
- HWDATA, HADDR and AHB control steering
- HBUSREQ and HGRANT arbitration

The SOC-Arbiter-AHB is used in AMBA AHB multi-master systems to arbitrate the access to the AHB bus. The SOC-Arbiter-AHB is basically a “traffic controller” which allows the AHB bus to be shared between multiple bus masters such as processors, dma controllers, and peripheral core master interfaces.

The SOC-Arbiter-AHB uses a round robin priority scheme with Master0 having the default priority. This priority scheme assures that each master equally has its turn at acquiring and completing an AHB bus transaction. Each inactive master is locked out (HLOCK) while the active master has access to the bus to prevent contention.

The SOC-Arbiter-AHB steers all the AHB HWDATA, HADDR, HTRANS, HWRITE, HSIZE and HBURST signaling from each master to the AHB system bus.

The SOC-Arbiter-AHB is delivered as a three master arbiter but can easily be configured to allow up to sixteen AHB bus masters.

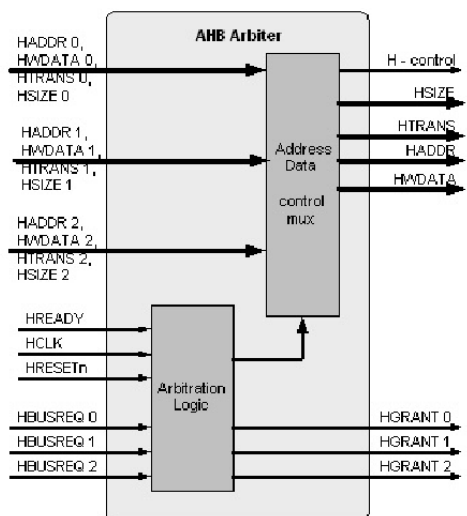
Deliverables

The SOC-Arbiter-AHB package includes fully tested and verified Verilog source. The SOC-Arbiter-AHB can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGAs.

Support

The SOC-Arbiter-AHB core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Block Diagram



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