



# SOC-Adec-AHB

## Address Decoder / Remap Core

### Features

- Scalable Address Decoder
- Hardware and software remap controls
- Invalid address detection
- AMBA AHB interface

The SOC-Adec-AHB is a fully scalable Address Decoder with a built in remap function to support multiple memory maps. The SOC-Adec-AHB generates separate enable signals for external devices such as FLASH and SRAM, internal memory, and various internal blocks. Datamux select signals are also generated to control which data is muxed onto the AHB data bus. The Address Decoder also detects and reports invalid addresses from the address bus.

The built-in remap logic is controllable through hardware and software. Hardware remap controls allow developers to force a memory map with a jumper connection. This is useful during system development and debugging where an in-circuit debugging system is used to boot from volatile memory. Software remap control allows for the system to be remapped on the fly during normal operation.

The SOC-Adec-AHB has an AMBA AHB interface.

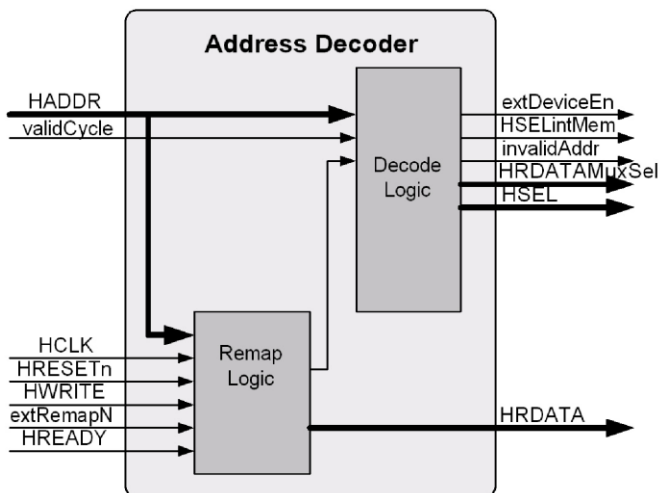
### Deliverables

The SOC-Adec-AHB package includes fully tested and verified Verilog source. The SOC-Adec-AHB can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGAs.

### Support

The SOC-Adec-AHB core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

### Block Diagram



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