



SOC-STNLCD-AHB

STN LCD Panel Controller Core

- ### Features
- STN LCD Panel Controller.
 - 16x32 Pixel FIFO.
 - 216 colors from available 65,536 color support via palette ROM.
 - Programmable frame rates.
 - Supports QVGA Panels.
 - Pixel DMA controller.
 - Programmable Interrupt Interface.
 - Supports wide variety of system clock rates

This configurable STN LCD Panel Controller IP core interfaces to an AMBA 2.0 AHB bus and provides all the timing control and pixel serialization for controlling various STN LCD Display Panels. It is designed for QVGA style STN-LCD Panels.

The controller modulates pixel information to generate panel colors using grayscale encoder logic. Pixel clock generation, frame control, and display controls are fully programmable and can be used with a wide range of system clock rates. Display information is held in system memory or external memory and is accessed by the core's AHB DMA controller. 16 bit pixels are accessed two words (32 bits) at a time and then serialized as 8-bit encoded color pixels. 16 bits (2 bytes) are used to create the 5,6,5 RGB pixel format. The core creates 2^5 , 2^6 , 2^5 grey scales for each RGB respectively, to support 65,536 colors. A 256-byte palette ROM selects the color map.

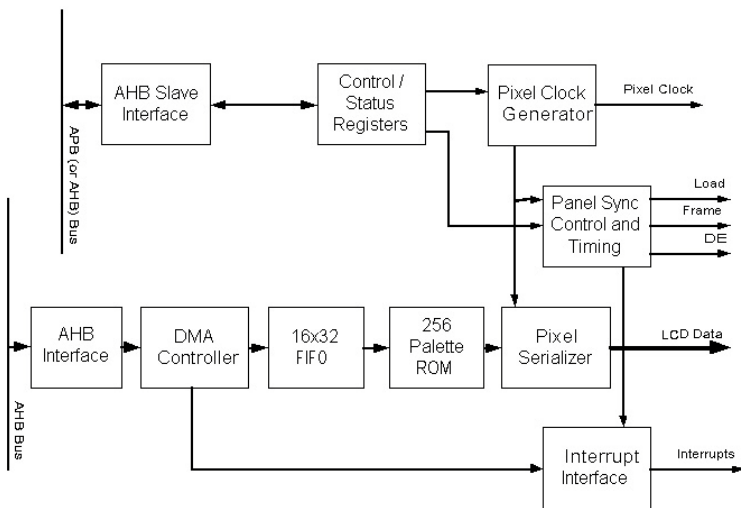
Interrupt sources timed to frame and control signals are programmable and selectable to signal the processor to update display information. The core is totally synchronous. All control and pixel timing is derived from the system clock input. The pixel clock and timing signals are programmable, allowing the STN-LCD Controller to be used with a variety of STN panels.

Display Data Organization

Pixel data is read from memory 32 bits at a time, or two 5,6,5 RGB pixels at a time. Pixel data is organized per word as shown.

Pixel 1, 32:16			Pixel 0, 15:0		
Blue	Green	Red	Blue	Green	Red
5 bits	6 bits	5 bits	5 bits	6 bits	5 bits
15:11	10:5	4:0	15:11	10:5	4:0

Block Diagram



Functional Description

AMBA 2.0 (AHB) Interface — Connected to the microprocessor bus through the AMBA bus interface signals. **DMA and FIFO Control** — The DMA (AHB master) reads pixel-organized data from a display frame buffer located either in internal memory or external memory. **Pixel Serializer** — Takes the data from the FIFO, through the Palette ROM, and presents it to the STN-LCD panel in a pixel serial fashion. **Panel Sync Control and Timing** — Generates all the synchronizing and pixel timing control for the STN-LCD panel. It generates Frame and Load signals based on the pixel clock. **Pixel Clock Generator** — The pixel clock is generated from the system clock divisor control register. **Interrupt Controller** — Interrupts are generated to the processor from the following conditions, which are enabled

under program control. FIFO status: Full, Half Full (watermark), or Empty.

Deliverables

The **SoC-STN-LCD Controller** package includes Verilog source and simulation test-benches. The **SoC-STN-LCD Controller** can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGAs.

Support

The **soc-SRAMCtrl-AHB** core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.